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Survey on FPGA Based Space Vector PWM Motion Control

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ABSTRACT: The Space vector Pulse Width Modulation (SVPWM) is possibly one of the best techniques among all the PWM techniques for variable voltage variable frequency drives. This is a direct digital technique and space vector concept is utilized to calculate the duty cycles of inverter switching devices. Rapid growth in VLSI technology and EDA techniques has given way for the development of complex and compact controllers for industrial control systems. Specific hardware technologies such as FPGAs based architecture platforms provide rapid prototyping, high performance signal processing and flexibility for implementation of drive, motion and activation control of drives. This paper reviews some of the FPGA based SVPWM motor control systems available in the literature.

KEYWORDS: space vector pulse width modulation, variable voltage variable frequency drives, revolving voltage vector, base vectors, sectors ,digital implementation, three phase voltage source inverter, FPGA based controllers

I. INTRODUCTION TO SVPWM

The Space Vector Pulse Width Modulation (SVPWM) method is an advanced PWM method and it is possibly one of the best among all the PWM techniques for variable frequency, variable voltage drives applications. In recent years, this method has gradually obtained widespread applications in power electronics and electrical drives, because of its superior performance characteristics. Compared to Sinusoidal Pulse Width Modulation (SPWM), SVPWM is more suitable for digital implementation. It is a sophisticated averaging algorithm which increases the obtainable DC voltage utilization ratio.A higher amount of AC side voltage is achieved with the same DC side voltage. In space vector theory three phase sine signals get transformed into a revolving vector with a constant magnitude and constant angular frequency. In Space vector PWM the revolving voltage vector is used as a voltage reference instead of modulating signals and the objective is to generate PWM load line voltages that are in an average equal to the given reference load voltage.

SVPWM technique attains this objective by switching the power semiconductor devices in a special sequence for example in a three phase voltage source inverter having six power semiconductors devices , the inverter can move through eight switching states. The switching states are determined by simple formulae that are easy to implement digitally.When employing a three phase inverter bridge, the phasormust be obtained by a combination of eight possible states. In order not to short-circuit the power supply, the high-side and low-side switches in any inverter legcannot be closed at the same time. This allows 8 possible combinations of the switch states. A combination is fully described by the high-side switch states, as the low-side corresponding switch states will be complementary. The eight possible combinations, when represented in the α/β plane, become eight space vectors, of which 2 are null vectors, as can be observed in Fig. 1. These base-vectors define a hexagon, and split it into 6 sectors. Main routines in SVPWM algorithm are

1. Determine reference phasor.
2. Determine duty cycles for base vectors.
3. Determine switching order of switches.
4. Generate PWM carrier and apply modulation.

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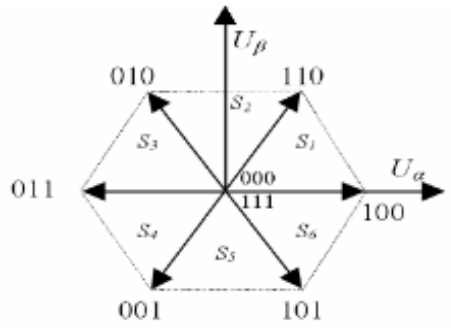

Figure 1: The base vector defined hexagon
This figure describes the eight switching states arranged in the hexagon

Advantages of SVPWM technique
This method offers improved bus utilization, maximum output voltage is 1.155 times more than with sine triangular PWM technique. Without going into over modulation the AC output voltage can be increased. It also offers less commutation or switching losses because it offers greater flexibility to optimize switching waveforms. Only one reference space vector is needed to generate three phase sine waveforms. SVPWM switching rules give less total harmonic distortion and shifted spectrum. This method decreases the current distortion and gives low steady state torque, flux and current ripple. More advanced vector control can be implemented using SVPWMas reference voltage is a two dimensional quantity.

II. METHODOLOGY

In this paper,section A describes a method to combine space vector and carrier based modulation and produce seven types of modulationstrategies implemented on FPGA platform.Section B has a technique to reduce the computational overheads of the SVPWM algorithm by introducing an intermediate variable.Section Cproposes multisampling space vectors in one switching period which results in improved performance of the voltage source inverter used in drives.Section D uses the SVPWM technique to control the servomotor system.Section E describes FPGA Based Implementation of Space Vector Modulated Direct Torque Control For Induction Motor Drives.Section F Paper focuses on the design of a low power and high performance FPGA based Digital Space Vector Pulse Width Modulation (DSVPWM) controller for three phase voltage source inverter. A new method is proposed to realize easy, accurate and high performance DSVPWM technique based on FPGA with low resource consumption and reduced execution time than conventional methods.Section G Work focuses onthe design of a low power and high performance VHDL basedSVPWM controller for three phase Induction Motor drives basedonFPGAs.

A. FPGA-Based SVPWM Trigger Generator for a 341 Voltage Source Inverter

Cleumar S. Moreira', Raimundo C. S. Freire', Elmar U. K. Melcher', Gurdip S. Deep', Sebastian Y. C. Catunda2, Raimundo N. C. Alves3

In this paper the architecture of a reconfigurable FPGA-based pulse width modulator for generating trigger pulses for a 3 phase voltage source inverter is presented This circuit is based on a mixture of the space vector approach and the carrier-based modulation method. This circuit is capable of 7 different predefined modulation strategies. This architecture permits inclusion of a new user-defined strategy. The modulator structure has been decomposed into different functional modules and described in Verilog-HDL. The resulting code has been compiled and simulated for a 2000 gate FPGA.PWM trigger pulses are generated by directly comparing the reference signals against each other. In the carrier-based modulation, a zero sequence component is added to the three sinusoidal reference signals, thus distorting the reference signals to eliminating the certain harmonic components from the inverter output voltage. By comparison of this distorted reference signal with the triangular carrier, different switching patterns, are generated in accordance with chosen zero sequence component.

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Structure of the Proposed Modulator

The **multiplier module** is used to multiply index **m** with data read from the sinusoidal module.In the **modulation module,** each of the values storedin the sinusoidal module are multiplied in the multipliermodule by the10-bit number representing the modulationindex and this gives the modulation signal which is compared with the carrier signal instant by instant. To thismodulating signal is then summed a zero sequence component using a finite state machine.The **delay module** has as inputs, the PWM pulses generatedas a result of the comparison between the referencesand carrier waveforms and identifies the positive andnegative transitions. For those input signals, which suffersimultaneous transitions, a delay (dead time) is introducedto avoid simultaneous operation or conduction of switchesin the same leg.In the **SVM** (Space Vector Modulation) **module** thecalls are made to the modulation, carrier and delay modules,supervising the communication and synchronizationoperations. The final command pulses are then generated.The input signals to this module correspond to the flagsand command pulses and the same are designed to supervisethe read/write operations of the internal variables thatare necessary for the configuration of the modulator. This paper presents design and implementation of a versatile FPGAbased space vector modulator. Thisconfiguration is coded in Verilog HDL describing aspects of synchronism and communication between modules.

B. An Efficient SVPWM Algorithm With Low Computational Overhead for Three-Phase Inverters Zeliang Shu, Student Member, IEEE, Jian Tang, YuhuaGuo, and JisanLian

This paper proposes and develops a compact algorithm ofspace vector pulsewidth modulation (SVPWM) for three-phase inverters. Simplified by the proposed method, the conventionalSVPWM is decomposed into fast integer operations entirelyby using an intermediate vector, which will properly counteract theredundant calculations of the remaining procedures. This conceptcan not only simplify a two-level scheme, but is also suited for multilevelimplementation. Since it can be implemented without anymultiplier or divider, the fast algorithm is especially suitable forfield programmable gate array applications. Then, an area and speed efficient IP-core based on this algorithm is built and tested.It ensures lower hardware resource usage, and at the same time,operates several times faster than some reported examples. Experimental results obtained from a dc–ac inverter prototype arealso presented to verify the viability and effectiveness of the proposedalgorithm.IP-core designbased on FPGA adopting the compact architecture requiresmuch less resource and provides faster operatingfrequency than the conventional scheme. This concept can be used for the simplification of multilevel SVPWM scheme also.Proposed algorithmcan also be used in software applications, such as DSPor micro-controller technologies, where the ability to accuratelygenerate SVPWM pattern at real-time is crucial.

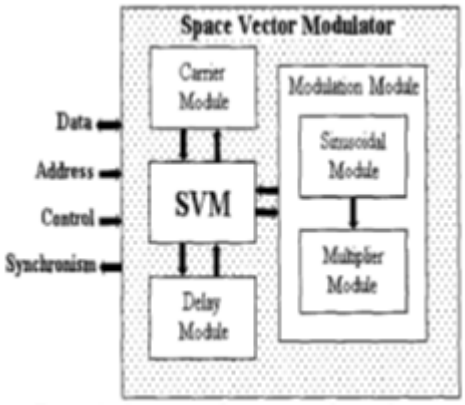

Figure 2: Structure of Proposed modulator:
This figure describes the various modules of the proposed modulator

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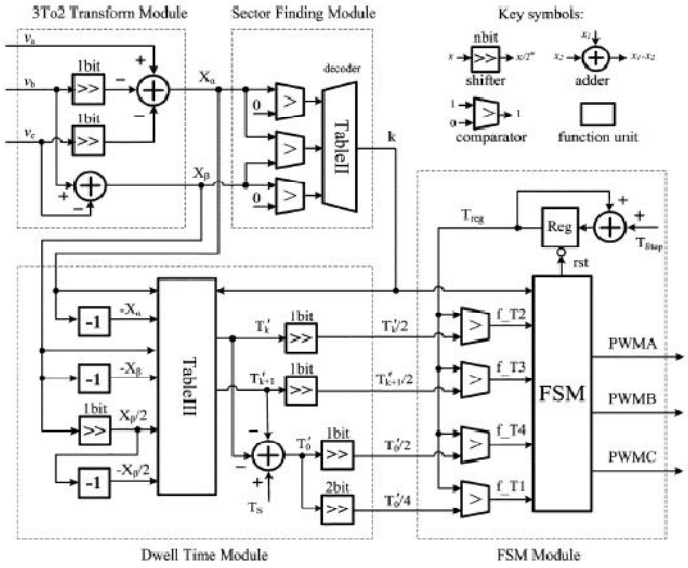

Figure 3: Compact architecture of the proposed SVPWM algorithm

C. **Three-Phase VSI with FPGA-Based Multisampled Space Vector Modulation**
Giovanna Oriti, Senior Member, IEEE, and Alexander L. Julian, Member, IEEE

This paperdemonstrates improved performance ofa three-phase voltage source inverter (VSI) when digital multi-sampled space vector modulation is used. The modulator and the inverter controller are implemented entirely using a field-programmable gate array platform, thus achieving increased bandwidth with respect to a typical digital signal processor or microprocessor-based controller. Increased controller bandwidth results in lower output voltage harmonic distortion in the frequency range above the fundamental and below the switching frequency. Experimental validation is presented together with the analysis carried out using a state space model of a VSI with an output LC filter.

Embedding space vector modulation in an FPGA creates an opportunity to recalculate the space vector timers multiple times during one switching period. This technique is often referred to as multiple sampling of the reference signal and can be implemented only if parallel computing is possible, as is the case with FPGA-based controllers.

This paper shows that the increased controller bandwidth, resulting from multiple sampling, is very beneficial for the output voltage quality. Bode plots created from simulations were used to understand the system gain and phase margins and tune the PI controller gains. Experimental time-domain and frequency-domain waveforms have showed the improved voltage quality of the VSI output voltage when 20 samples per period are used compared to typical double update space vector modulation.

D. Design and Implementation ofSVPWM Servo Control System Based on FPGA
Pang Haiyan, Xie Yun, Xiao Shanshan, Chen Bingcheng

The SVPWM servo control system described in this paper usesAltera's Cyclone II series FPGA chips, the correspondingFPGA development software platform is QuartusII7.2.QuartusII7.2 development platform includes HDL code input,component symbols input and circuit design and simulationEDA software embedded and other parts, in which functionalsimulation and timing simulation of the entire system designstage is the crucial phase, it can identify system design problems assoon as possible.

A hardware implementation method of SVPWM is shown, which lies in the calculation of the twoaxisstator voltage component, and then transforms into a threeaxisfrom 2-axis component of modulation component (throughthe coordinate transformation) the outputwaveform is converted to the best pulse width modulated signalthrough the

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adjusted SVPWM converter, the modulation signalentering the latch circuit can be set for the process of addingdead delay time the final modulated waveform is then used to control the three-phase inverter circuit.

The SVPWM Servo Control System involves thecalculation of pulse time and the sinusoidal signal generation,so numerical calculation and the calculation median must betaken into account. As the floating-point computationalcomplexity is high, the system has used integer arithmeticinstead, later when it is improved, it can be enhanced from 8-bit to 12-bit, l6-bit even to 32-bit. This design of servo-controlsystem has used 8-bit integer arithmetic, the values of sinereference tables are stored in the EPROM inside the FPGA.

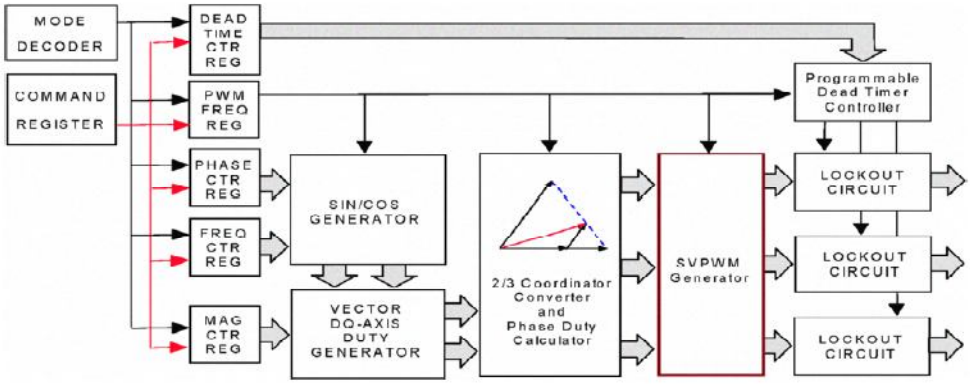

Figure 4: SVPWM digital servo Control system based FPGA
This figure describes the design of the digital servo system based on FPGA

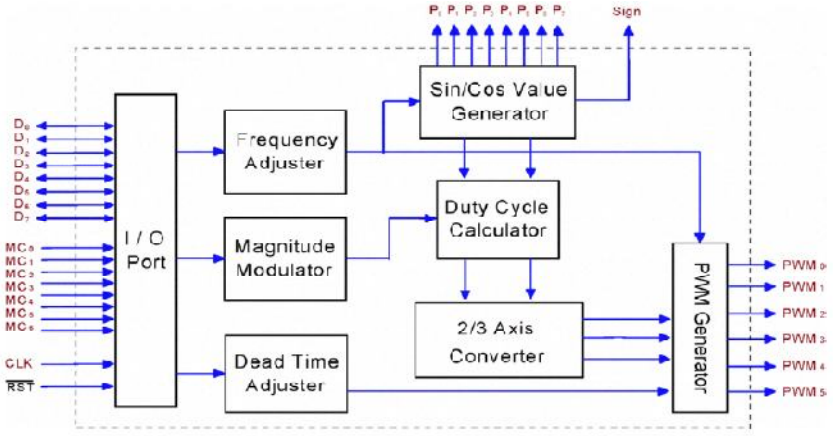

Figure 5: SVPWM control Module
This figure describes SVPWM control module that includes Frequency Adjuster,Magnitude Modulator, Dead Time Adjuster, Sin/Cos valuegeneration, Duty Cycle Calculator , 2/3 Axis Converter

E. FPGA Based Implementation of Space VectorModulated Direct Torque Control For InductionMotor Drive

R.Rajendran, Senior Member IACSIT and Dr.N.Devarajan

In this papera flexible, high computation speedand cost effective field programmable gate array (FPGA) based space vector modulated (SVM) direct torque control for an induction motor is presented.Direct Torque Control (DTC) using space vector modulation is shown to have the low steady state torque ripple, flux ripple and current distortion that is characteristic of space vector modulation and fast transient performance that is characteristics of direct torque control. This system has been implemented on the Xilinx Spartan 3E FPGA.The proposed method has the control objective of

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selecting the exact stator voltage vector that changes stator flux to meet the load angle reference and hence the desired torque while keeping flux amplitude constant .A space vector modulation algorithm is used to apply the required stator voltage vector. System is illustrated by the control system block diagram below.

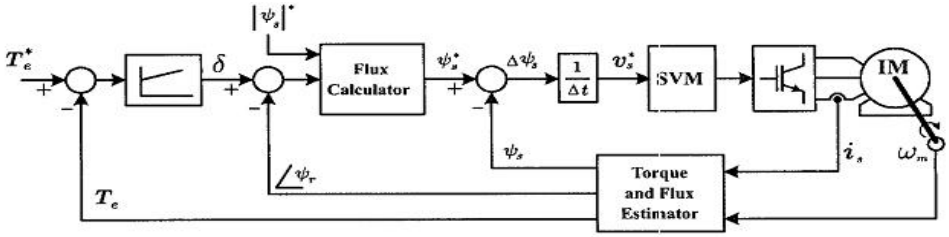

Fig 6: Direct Torque Control setup

A low cost Xilinx Spartan 3E FPGA, that contains 4,00,000 logical gates and works at 50 MHz(clock period equal to 20ns), was used as target component for the implementation of this controller.By implementing this controller in an FPGA, very good performance is reached, thanks to the inherent parallelism of FPGA-based solutions and their great flexibility to achieve different control functions.

F. High Performance FPGA Based Digital Space Vector PWM Three Phase Voltage Source Inverter
BahramRashidi,MehranSabahi

This paper focuses on the design of a low power and high performance FPGA based Digital Space Vector Pulse Width Modulation (DSVPWM) controller for three phase voltage source inverter. A new method is proposed to realize easy, accurate and high performance DSVPWM technique based on FPGA with low resource consumption and reduced execution time than conventional methods. Equations of SVPWM are relatively complicated and need a considerable time to execute on a typical microcontroller, therefore a simple method is presented to minimize run time of instructions,Proposed digital design for sector determination implements Rules based on simple and low power logic circuits, proposed design is based on combinational logic circuits thus there is increased performance and reduced power consumption. This proposed digital circuit implements sector determination completely and accurately. For increasing performance of design sub-pipelining technique can be used. The advantages of this technique over the other literatures include flexibility, high accuracy and reduced area. Therefore a simple method has been presented to change complicated SVPWM equations to a collection of shift, add and other similar uncomplicated orders to minimize run time of instructions. Proposed method has high performance, Stress Reduction, low power and high accuracy. To verify the proposed design a laboratory prototype has been arranged using of cyclone II FPGA board, an optical interface as IGBT drivers of voltage source inverter with an induction motor output load. Laboratory experiments and Xpower analyzer results demonstrate that, because of reduced hardware usage percentage, easy and fast instructions, proposed method has better performance and less power consumption than others works.Total power consumption of controller is reduced to 37 mW at 100MHz clock frequency.

G. FPGA Implementation of SVPWM Control Technique for Three Phase Induction Motor Drive Using Fixed Point Realization
ChaurasiyaRohit B., Mukesh D. Patil, Divya Shah1and Abhijit Kadam2 Electronics Engineering RamraoAdik Institute of Technology Nerul, Navi Mumbai

This work focuses onthe design of low power and high performance VHDL basedSVPWM controller for three phase Induction Motor driveonFPGAs. The integer realization of software part results in largenumber of subroutines thus utilizing large hardware resourceson FPGA board leading to more power consumption. Also dueto large code density the computational time is more. In thiswork the software part is implemented with proposed fixed pointrealization which increases the accuracy, also since there areno subroutines, it reduces total area on FPGA board. The codedensity is less, thereby decreasing computational time and powerconsumption. The simulation results for SVPWM generatedsignals are also given in this work. To prove the effectiveness ofthe proposed method the hardware utilization by the proposedmethod are compared with integer realization.

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It is observed that, the fixed point implementation requires less hardware, improves accuracy and makes the implementation simpler as compared to integer realization.

III. CONCLUSION

With rapid progress in VLSI technology the development of efficient motor control systems has also made major progress. Many of the motor drives in use have DSP based digital control strategy,this has the advantage of simple software control and flexibility. However recent devices like FPGAs provide rapid prototyping, high performance signal processing and flexibility due to their reconfigurable architecture.In particular an FPGA-based SVPWM modulator can take multiple samples of the reference voltage and recalculate the power converter switching states and timers several times over one switching period which is an advantage over DSP based controllers.However, in many cases, the design of FPGA-based controller architectures is rather intuitive and requires the designer to master different areas (micro-electronics, control, and electrical machine theories). It is particularly true for complex algorithm structures such as the ones found in drive control applications.This paper makes an attempt to survey the techniques present in the literature for FPGA based space vector modulated motor control systems.

FUTURE SCOPE

The FPGA based design of SVPWM can be extended for low Power realization, and also to improve power speed product of FPGAs. This discussion also lays the of foundation of analyzing motor control systems based onSOC(system on chip) specialization for the future.

REFERENCES

1. Y. Tzou and H.-J. Hsu, “FPGA realization of space-vector PWM control IC for three-phase PWM inverters,” *IEEE Trans. Power Electron.*, vol. 12, no. 6, pp. 953–963, Nov. 1997.
2. M. Tonelli, P. Battaiotto, and M. I. Valla, “FPGA implementation of an universal space vector modulator,” in *Proc. IEEE IECON*, 2001, vol. 2, pp. 1172–1177.
3. S. Chen and G. Joos, “Symmetrical SVPWM pattern generator using field programmable gate array implementation,” in *Proc. IEEE APEC*, 2002,1004–1010. |
4. R. Walker, “Digitally-implemented naturally sampled PWM suitable for multilevel control,” *IEEE Trans. Power Electron.*, vol. 18, no. 6, 1322–1329, Nov. 2003.
5. Z. Zhou, T. Li, T. Takahashi, and E. Ho, “Design of a universal space vector PWM controller based on FPGA,” in *Proc. IEEE APEC*, 2004, vol. 3, pp. 1698–1702.
6. G. Yang, P. Zhao, and Z. Zhou, “The design of SVPWM IP core based on FPGA,” in *Proc. IEEE Embedded Softw. Syst. Symp.*, Jul. 2008, pp. 191– 196.
7. W. Chen, C. Pien, and Y. Feng, “Design of an FPGA-based space vector PWM generator for three-phase voltage-sourced inverters,” in *Proc. IEEEPower Energy Conf.*, Dec. 2008, pp. 584–588.
8. S. Berto,A.Paccagnella, M. Ceschia, S. Bolognani, and M. Zigliotto, “Potentials and pitfalls of FPGA application in inverter drives—A case study,” in *Proc. IEEE ICIT*, 2003, pp. 500–505.
9. L. Corradini and P. Mattavelli, “Analysis of multiple sampling technique for digitally controlled DC–DC converters,” in *Proc. PESC*, 2006, pp. 1–6.
10. L. Corradini and P. Mattavelli, “Modeling of multisampled pulse width modulators for digitally controlled DC–DC converters,” *IEEE Trans Ind.Electron.*, vol. 23, no. 4, pp. 1839–1847, Jul. 2008.
11. L. Julian and G. Oriti, “FPGA based digital implementation of naturally sampled space vector modulation,” in *Proc. IEEE ECCE*, San Jose, CA, Sep. 2009, pp. 625–630.
12. K. Lee, I. T. Wallace, and A. S. Bhadkamkar, “Design oriented analysis of DC link current observer of a three-phase double conversion un interrupt-able power system or adjustable speed drive,” in *Proc. IEEE Appl. PowerElectron. Conf.*, 2007, pp. 598–605.