Volume 2, No. 2, February 2011
Journal of Global Research in Computer Science
ISSN-2229-371X
REVIEW ARTICLE
Available Online at www.jgrcs.info

Comparison between Low Power Clock Distribution Schemes in VLSI Design

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Abstract: In the VLSI design low power is very important aspect at different level of designing. In this paper it is tried to review different factors affecting the power dissipation due to various clock distribution schemes like as single driver clock scheme and distributed buffers clock scheme. There are different tradeoffs in both of techniques such as size of buffers, number of buffers etc. Here it is also tried to showing various effects of particular clock distribution scheme such as clock skew, clock jitter.
Keywords: Single driver clock scheme, Distributed buffer scheme, Clock jitter, Clock skew.

INTRODUCTION

CMOS digital systems are approaching to Gigahertz frequency range. It is the result of submicron technology. At the same time power dissipation due to high frequency, global warming, environmental issues, battery durability requirement and light weighted problem have become a very important factor in VLSI industry. In the VLSI physical design step routing is also having a considerable role which require more and more attention to minimize power consumption.

For providing synchronization of the digital system one or more reference clocks are used. Fully synchronization is done by using common clock. By using a single clock all parts of digital system is clocked for their different operations. Clock tree used for globally distribution the clock signal to all modules. Power dissipation in CMOS is characterized by short circuit power dissipation and dynamic power dissipation. Short circuit power dissipation is power dissipated during switching interval between NMOS & PMOS. Dynamic power dissipation is due to charging and discharging capacitor. Due to high frequency used in recent technology switching activity increase, resulting it large load introduced. Hence clock is the major source of dynamic power dissipation. Dynamic power dissipation by switching of clock is given by:

$$P_{clk} = V^2_{dd}.f.(C_L + C_D) \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

Where C_L is Total load capacitance on clock which is given by

$$C_L = N.C_g + 1.5(2^h-1).C_W + \alpha\,(4^h.N.C_W)^{1/4} \quad \ldots\ldots\ldots\ldots (2)$$

Where N=Number of clock terminals.
C_g = Capacitance at each terminal.
H = Level of clock routing.

D= Chip dimension.

α = Estimation factor depending on routing algorithm.
This means, Dynamic power of clock increase on increasing chip dimension, number of clock devices, load capacitance and wire capacitance, driver capacitance.
There are two type of problems in clock generation
a) **Clock skew**: This is the variation in delay from clock source to clock destination in different clocks that is shown in fig 1

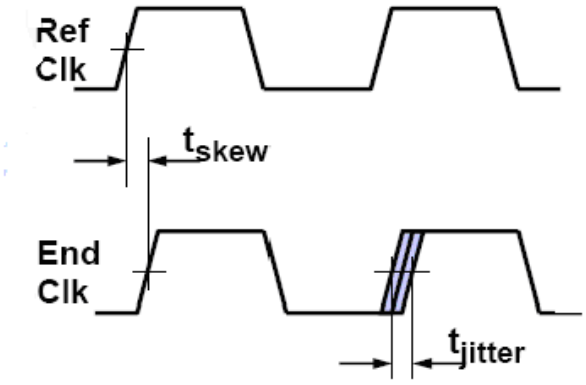

Figure.1 Clock skew problem

(b)**Clock jitter** is defined as temporal variation of clock with respect to reference edge. It is of two type long jitter and cycle to cycle jitter. The above both of problems are minimize by using good appropriate clock scheme either single or distributed buffer. Fig 2 shows the different sources of clock skew.

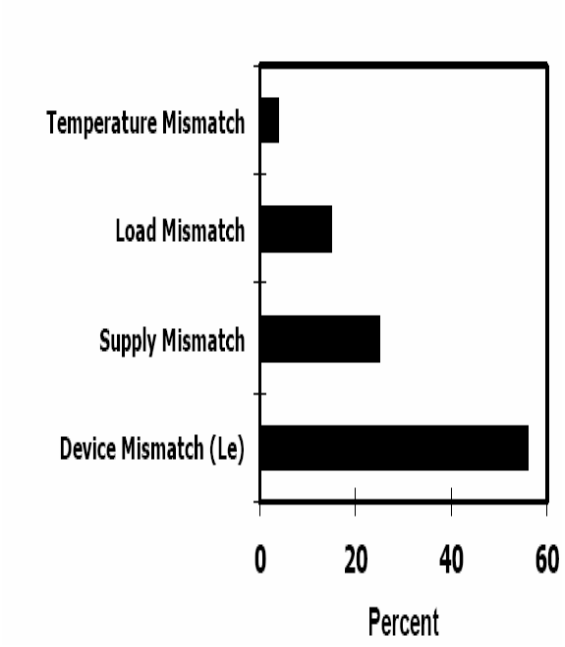

Figure.2 Sources of clock skew

SINGLE BUFFER

Buffers are used in clock schemes to drive load capacitance and fast tansitions. The single driver scheme has the advantage of avoiding the adjustment of intermediate buffer delay as in distributed buffer schemes. Often in conjuction with this scheme, wire sizing is used to reduce the clock phase delay. Widening the branches that are closed to clock source can also reduce clock source skew caused by asymmetric clock tree load and wire with deviations. If the interconnect resistance of the buffer at the clock source is small as compared to the buffer output resistance, it is called as single driver clock scheme.

DISTRIBUTED BUFFER SCHEME

In this, intermediate buffers are inserted in the various part of clock tree. Advantage of using small buffer is flexible to place for save layout. Here clock skew and phase delay is reduced by intermediate buffers. This is the most common and general approach to equi-potential clock distribution scheme. It leads to an asymmetric structure. All paths are balanced in the distributed buffer scheme as shown in fig 3.

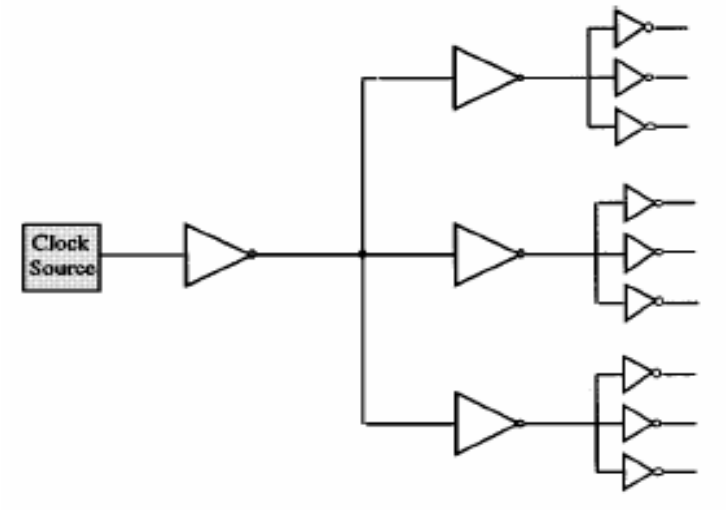

Figure.3 Distributed buffer scheme

Intermediate small buffer and wire widening is used to reduce delay. But wire widening require large size of buffer at source. In single driver short circuit power dissipation is more than distributed buffer scheme due to the reason of small buffer used in distributed buffer scheme.

There are various trade offs between both of clock distribution schemes which are shown in the following table. Appropriate technique is used according to available layout area, complexity of the system, calculating parasitic capacitance effect of individual clock scheme on the whole system etc.

Factors	**Clock schemes**	
	Single Driver	**Distributed Buffer**
Wire widening	Allowed	Not allowed
Short circuit power dissipation	More	Few
Intermediate buffer adjustment	Not required	Required

Figure.4 Comparison table

Clock line can also be treated as RC delay lie as shown in fig 5.

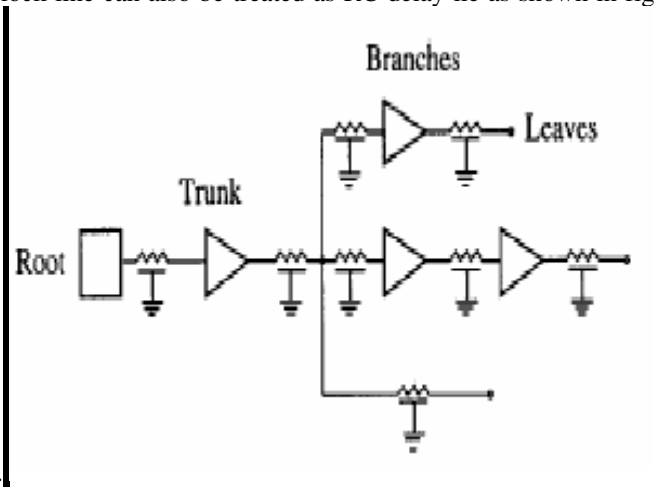

Figure 6 Clock line treated as RC delay line

Clock skew between source s1 and s2 is given by

$$Ts=R_{L1}.C_{L1}/w_1 - R_{L2}.C_{L2}/w_2 \quad \text{.....(3)}$$

Without wire width variation skew is linear function of path length and with wire width variation skew is linear function of product of path length and load capacitance. Hence if wire width increase clock skew decrease but here load capacitance is increase then power dissipation increase. So decrement in power dissipation is done by both path delay and load decreasing.

Buffer size can be minimize for reducing power dissipation. It can be formulated as- given a clock tree T, intermediate buffer is inserted by insertion algorithm, the problem of power minimization by buffer sizing(PMBS) is determine buffer size in T, to minimize total power subject to phase delay constraint d_p and skew constraint $t^b_{s.}$

CONCLUSION

Here it is tried to specify the different needs of clock schemes. Different problems in clock like clock jitter, clock skew is also incorporated when clock is designed. These problems are eliminated by using different clock schemes which have different tradeoffs. According to requirement appropriate technique is used.

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