

A Novel Control Algorithm for Conversion of AC-DC with Improved Power Factor and Efficiency

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ABSTRACT:A Single power-conversion ac–dc converter with high power factor and high efficiency. The proposed converter is derived by integrating a full-bridge diode rectifier and a series-resonant active-clamp dc–dc converter. To obtain a high power factor without a power factor correction circuit, this paper proposes a novel control algorithm. The proposed converter provides single power-conversion by using the novel control algorithm for both power factor correction and output control. Also, the active-clamp circuit clamps the surge voltage of switches and recycles the energy stored in the leakage inductance of the transformer. Moreover, it provides zero-voltage turn-on switching of the switches. Also, a series-resonant circuit of the output-voltage doubler removes the reverse-recovery problem of the output diodes. The proposed converter provides maximum power factor 0.995 and maximum efficiency of 95.1% at the full load.

KEYWORDS:Active-clamp circuit, series-resonant circuit, single power-conversion.

I.INTRODUCTION

GENERALLY, the ac–dc converter consists of a full-bridge diode rectifier, a dc-link capacitor and a high frequency dc–dc converter. These converters absorb energy from the ac line only when the rectified line voltage is higher than the dc link voltage. Therefore, these kinds of converters have a highly distorted input current, resulting in a large amount of harmonics and a low power factor. To solve the harmonic pollution caused by ac–dc converters, a number of power factor correction (PFC) ac–dc converters have been proposed and developed[1]-[8] . The PFC ac–dc converter can be implemented by using two power-processing stages. The PFC input stage is used to obtain high power factor while maintaining a constant dc-link voltage. Most PFC circuits employ the boost converter . The output stage, which is a high frequency dc–dc converter, gives a desired output. Two power-processing stages require each control circuit consisting of gate drivers and those controllers. In general, the PFC ac–dc converter can be categorized into two types: two-stage ac–dc converters and single stage ac–dc converters. Two-stage ac–dc converters consist of two power-processing stages with their respective control circuits. However, two-stage ac–dc converters raise power losses and the manufacturing cost, eventually reducing the system efficiency and the price competitiveness. In efforts to reduce the component count, the size, and the cost, a number of single-stage ac–dc converters have been proposed and developed. The main idea is that a PFC input stage and a high frequency dc–dc converter are simplified by sharing common switches so that the PFC controller, the PFC switch, and its gate driver can be eliminated. .

II.CONVENTIONAL METHOD

Fig. 1(a) shows the schematic diagram of the conventional two-stage ac–dc converter. It comprises a full-bridge diode rectifier, a PFC circuit, a control circuit for the PFC circuit, a high frequency dc–dc converter, and a control circuit for output control. The control circuit is composed of gate-drivers and a controller. Namely, two-stage ac–dc converters have two power processing stages with their respective control circuits. Also, the boost type PFC converter used in most PFC input stages requires the dc-link electrolytic capacitor and the inductor. Two control circuits, the dc-link capacitor and the inductor raise the size, weight and the cost of the converter and reduce the price competitiveness. On the other hand, the advantage is to decouple control of the dc-link capacitor voltage from that of the output voltage and

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

realize much tighter output control. However, the single stage ac-dc converters have several disadvantages. First, the power factor is also related to the controller, indicating that the variation of the load or the input voltage will change the power factor. Second, the output voltage control bandwidth is limited to a few hertz not to excessively distort the input current. Third, single-stage ac-dc converters require the dc-link electrolytic capacitor and the inductor for the PFC circuit, just like two-stage converters. Finally, the conventional single-stage ac-dc converters have high voltage stresses or low power factor.

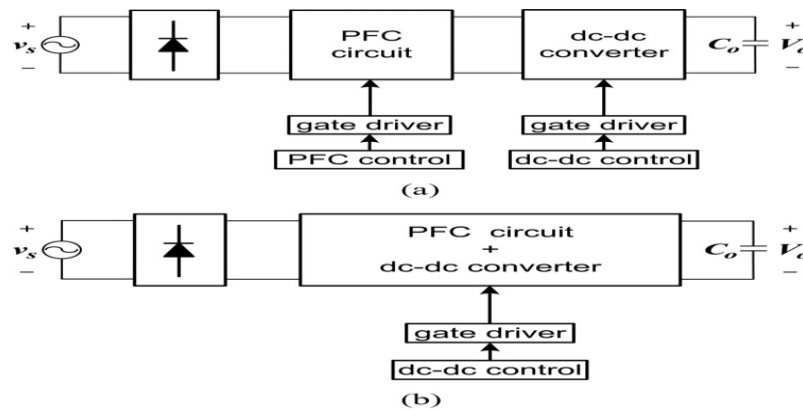


Fig. 1. Block diagrams of the conventional PFC converter (a) Two-stage converter. (b) Single-stage converter.

III. PROPOSED METHOD

Fig.2. shows the schematic diagram of the single power-conversion ac-dc converter. It consists of a full-bridge diode rectifier, a high frequency dc-dc converter, and a control circuit. That is, the single power-conversion ac-dc converter has also one control circuit because it has no PFC circuit. However, it requires the control algorithm for both PFC and output control, unlike single-stage ac-dc converters. Also, it has a large ac second-harmonic ripple component reflected at the output voltage in comparison with two-stage and single stage converters because it has no dc-link electrolytic capacitor. However, the single power-conversion ac-dc converter provides a simple structure, a low cost, and low voltage stresses because it has no PFC circuit composed of the inductor, power switching devices and the dc-link electrolytic capacitor. Therefore, the single power-conversion ac-dc converter is preferred option when the cost per unit is more important concerns than reliability.

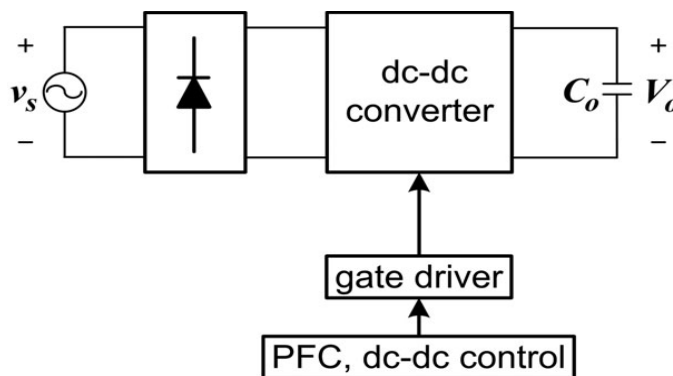


Fig.2. Proposed Single Power Conversion Converter

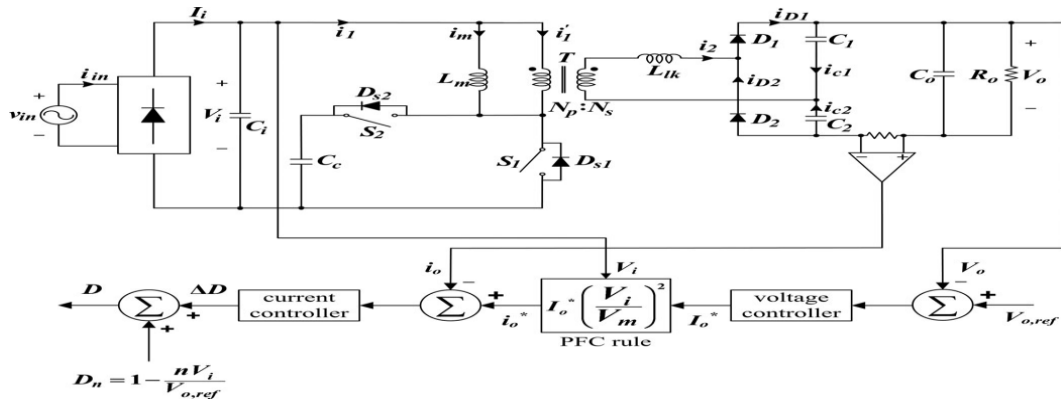


Fig. 3. Proposed single power-conversion ac-dc converter and the control block diagram.

The operating modes of the input side and the output side are shown in Figs. 4 and 5, respectively. The rectified input voltage

$$V_i \text{ is } |v_{in}| = |V_m \sin \omega t| \dots \dots \dots 1$$

where V_m is the amplitude of the input voltage and ω is the angular frequency of the input voltage. Prior to Mode 1, the primary current i_1 is a negative direction and the secondary current i_2 is zero.

Mode 1 [t_0, t_1]: At the time t_0 , the voltage v_{s1} across S_1 becomes zero and D_{s1} begins to conduct power. After the time t_0 , S_1 is turned on. Since i_1 started flowing through D_{s1} before S_1 was turned on, S_1 achieves the ZVS turn-on. As shown in fig.4

$$i_o(t) = i_2(t) - i_{c1}(t) = 1/2 i_{D1}(t) \dots \dots \dots 2$$

Mode 2 [t_1, t_2]: At the time t_1 , i_1 changes its direction to positive. L_{lk} and C_r still resonate similar to Mode 1.

Mode 3 [t_2, t_3]: At the time t_2 , i_2 becomes zero and D_1 is maintained in the on-state with the zero current. I_1 and i_m are equal during this interval. Therefore, i_1 terminates the first resonance and increases linearly as (1).

Mode 4 [t_3, t_4]: At the time t_3 , S_1 is turned off and D_1 is turned off with the zero current. The ZCS turn-off of D_1 removes its reverse-recovery problem. The voltage v_{s2} across S_2 becomes zero and the body diode D_{s2} begins to conduct power. After the time t_3 , the ZVS turn-on of the auxiliary switch S_2 is achieved.

Mode 5 [t_4, t_5]: At the time t_4 , L_{lk} and C_r still resonate similar to Mode 4. In addition, i_1 may change its direction during this interval based on the designed resonant frequency. At the time t_4 , L_{lk} and C_r still resonate similar to Mode 4. In addition, i_1 may change its direction during this interval based on the designed resonant frequency f .

Mode 6 [t_5, t_6]: At the time t_5 , i_2 becomes zero and D_2 is maintained to the on-state with the zero current. i_1 and i_m are equal during this mode. Therefore, i_1 terminates the series resonance and decreases linearly as (9). At the end of this mode, D_2 is turned off with the zero current. The ZCS turn-off of D_2 removes its reverse-recovery problem.

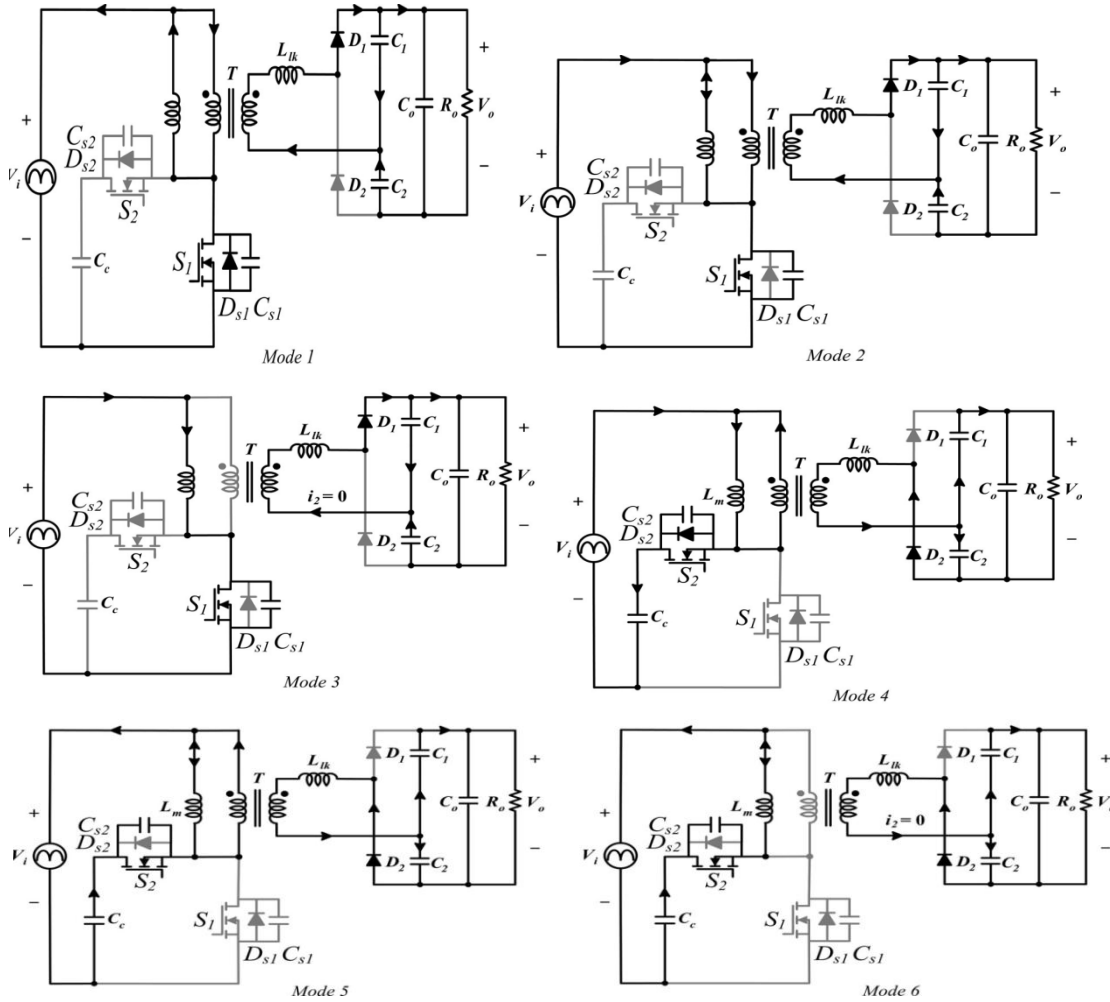


Fig4: Operating modes of the proposed ac–dc converter.

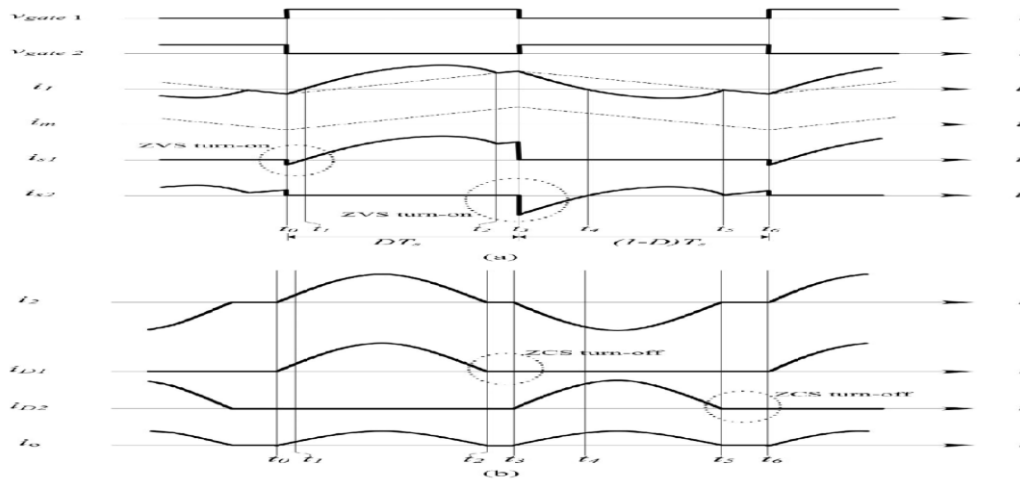


Fig. 5. Theoretical waveforms of the proposed converter. (a) Input side waveforms. (b) Output side waveforms.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 5, May 2015

IV. CONTROL ALGORITHM

The proposed converter has no PFC circuit. Therefore, to obtain a high power factor, it requires the control algorithm for both PFC and output control. The duty ratio D according to the input current i_{in} is hard to control because the relation of D and i_{in} is nonlinear. To achieve good controllability, the nonlinear system needs to be transformed into the linear system by the feedback linearization.

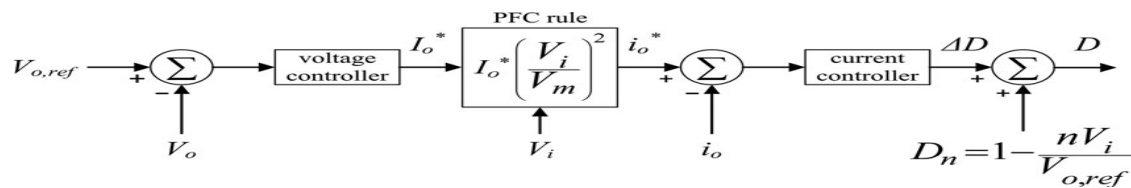


FIG6: CONTROL BLOCK DIAGRAM OF THE PROPOSED CONVERTER

Fig. 6 shows the control block diagram of the proposed converter. The voltage controller attempts to minimize the error value as the difference between V_o,ref and the measured output voltage by adjusting i_o^* that is, i_o^* is calculated by the voltage controller, and then i_o^* is calculated by the PFC rule in Fig. 6. In order to realize the PFC rule, synchronization with input voltage v_{in} is necessary. Since V_i includes the information about the amplitude and the phase of v_{in} , the synchronization with v_{in} is implemented by using V_i as shown in Fig. 2.

The current controller attempts to minimize the error value as the difference between i_o^* and the measured output current i_o by adjusting ΔD . Finally, D is obtained by adding ΔD to D_n . The proposed control system consists of the inner loop and the outer loop. The inner loop is the current control loop and the outer loop is the output voltage control loop. The proposed control system is analyzed by using a small signal model. The crossover frequency of the open-loop transfer function $T_v(s)$ for the voltage controller is chosen much smaller than the open-loop transfer function $T_i(s)$ for the inner current loop. The open-loop transfer functions $T_i(s)$ and $T_v(s)$ are expressed as

$$T_i(s) = H_i \cdot C_{ic}(s) \cdot G_{id}(s) \dots\dots\dots 3$$

$$T_v(s) = H_v \cdot C_{vc}(s) \cdot G_{vi}(s) \dots\dots\dots 4$$

where $H_i(s)$ and $H_v(s)$ are current sensor gain and voltage sensor gain, respectively. The small signal transfer functions of the duty ratio-to-output current and the output current-to voltage, respectively, can be obtained as follows

$$I_o^* = I_o^* (V_i/V_M)^2 \dots\dots\dots 5$$

V. SIMULATION AND RESULTS

A simulation design of minimization method for single phase inverter without an output filter is implemented in MATLAB/ SIMULINK with the help of wing energy, boost rectifier, universal bridge, controllers and FFT as shown in figure 8

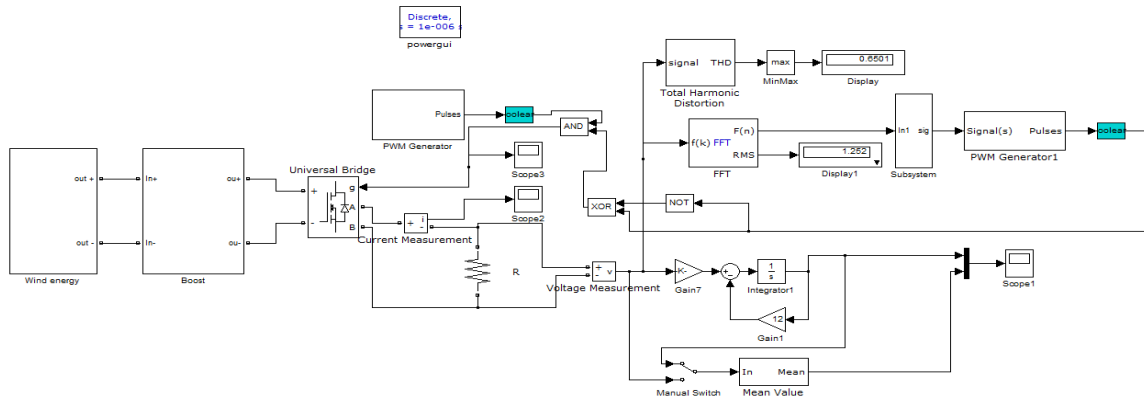


Fig. 8 Simulation model

The output waveform of inverter output as shown in figure 10a. When manual switch is connect directly to the output of inverter, there is a dc voltage of 1 V appears at output. After switch connected to PI, the output voltage is minimized as shown in figure 10b.

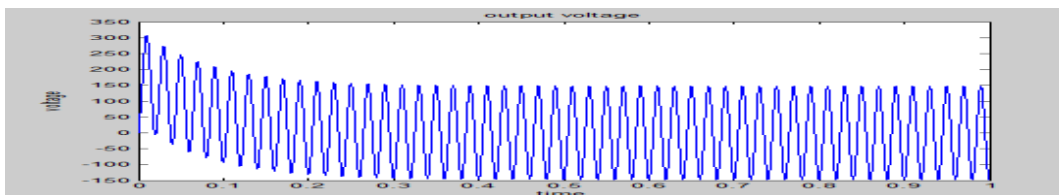


Fig9(a)

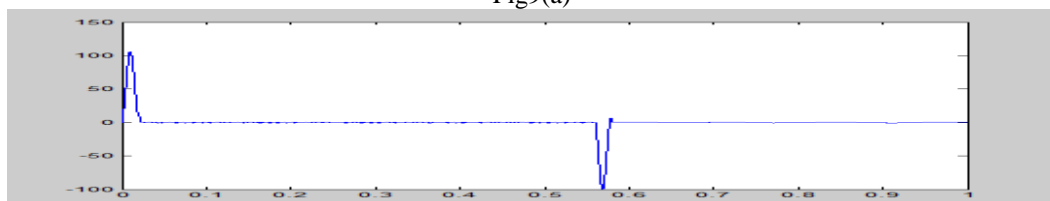


Fig9(b)

← Before switch connected to PI controller
→ With PI controller →

Fig. 9 Output voltage of inverter: a) Inverter output voltage, b) dc at output voltage

The THD value can be obtained by using FFT analysis, as shown in figure 11 and frequency spectrum of proposed system as shown in figure 12. Both are clearly shows harmonics are minimized and THD obtained is 4.24% , complies with the limit imposed by the standards.

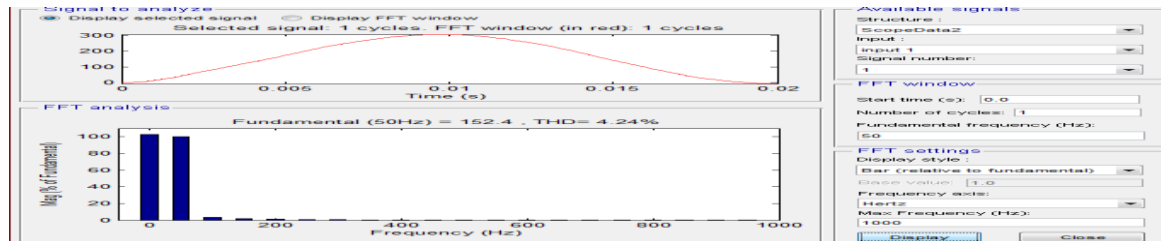


Fig. 10. FFT analysis

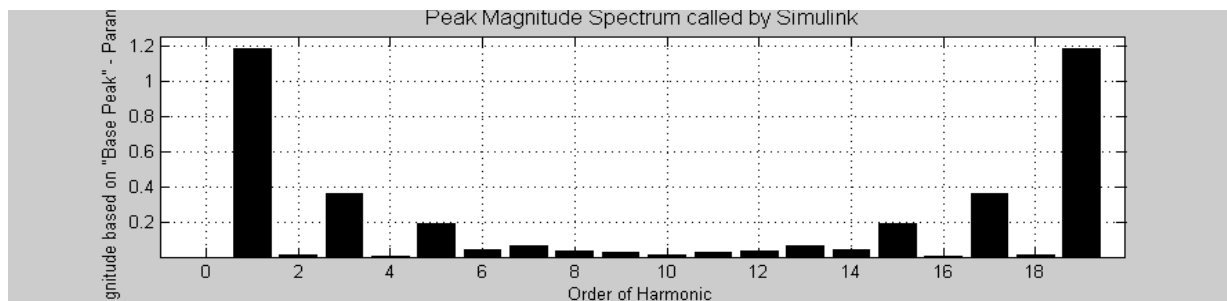


Fig 11: Frequency spectrum

VI. CONCLUSION

A novel approach to harmonic minimization method for single phase inverter established on mirror injection of harmonic and elimination of dc principle has been proposed. The following conclusions can be drawn after the imaginary analysis and the experimental results reported in this paper the proposed system minimizes the harmonics generated by the switching operation as well as harmonics generated by dc nature of the source and external point i.e. grid. Improvement of THD, through the cancellation of low-order harmonics and minimization of dc, so that the output voltage complies with the limit imposed by the standards, without the use of a filter.

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