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Wireless ECG monitoring system with remote data logging using PSoC and CyFi

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ABSTRACT: This work proposes design of a low power sensor node which acquires ECG signal, process and transmits it over wireless medium. Programmable System on Chip (PSoC) processor performs rapid, complex signal processing and consumes low power. These PSoC's capabilities extend its use in designing intelligent wireless sensor node. ECG detection and processing system detects R peaks at regular intervals, calculate heart rate and classify it. High accuracy, low error rate and good noise immunity is achieved by simple thresholding technique. For longer sensor node life, power consumption plays a very essential role. Instead of logging data continuously to the base station, intelligent sensor node enables transmitter only when critical heart rate is observed. Further reduction in power consumption is achieved by using low power CY3271 sensor node itself. Power analysis shows reduction in power due to reduced transmission rate. This results in low traffic over the network.

Keywords: ECG detection and processing system, logging, intelligent sensor, thresholding, CY3271 sensor node.

I. INTRODUCTION

Wireless sensor networks (WSNs) consist of number of sensor nodes. These nodes can be deployed especially in regions where remote monitoring is not possible. Regions can be thick forest, inaccessible terrains or areas affected by disaster. With evolution in fabrication technologies, size of devices have become smaller, consume less power and are priced low. This motivation has made size of the sensor node to shrink, with extending its computation capabilities. Number of such small sensor nodes can be deployed in a large region. Because of their increased capabilities, these nodes can hop data to their neighbouring node using advanced network protocols. Data can be sent to any distant node through these clustered nodes. These nodes together perform large data processing activities at very low power. Putting together, WSN's provide advantages like flexibility, fault tolerance, high sensing fidelity at low cost [1]. Rapid deployment characteristics of sensor networks fancy their use in remote patient monitoring system and sports training facilities. Remote care helps to measure vital body signals such as blood pressure and body temperature from a remote distance.

Advantages of WSN have helped to design Body Sensor Network technology (BSN). BSN consists of number of sensors attached on different areas of body called Body Area Network (BAN) [2]. These sensors individually collect data and transmit to the remote clinics or hospitals. This technique is very much helpful for elderly patients who face difficulty in visiting hospitals regularly and long term monitoring is recommended. Adhesive electrodes cannot be used for long term ECG monitoring. Nodes with non contact electrodes [3-5] are preferred for such patients. ECG monitoring system designed using microcontrollers require external amplification and filter circuits to acquire ECG signal. Thus, increase power consumption.

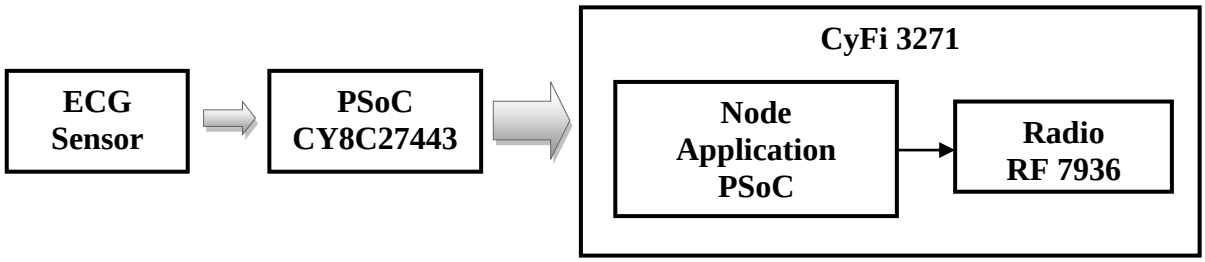

Fig. 1 PSoC interface with sensor node.

This paper presents a novel approach of interfacing a highly versatile Programmable System On Chip (PSoC) with wireless sensor node CY 3271 sensor node, both from Cypress semiconductors [12], [13]. This interface is shown in Fig. 1. PSoC enables greater integration, good power efficiency and higher accuracy at lower price. A PSoC mixed signal array is a low power programmable Systems on Chip (SoC). This allows configuring, programming of analog and digital components that are typically used in embedded systems. It also has a built in microcontroller which

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integrates and controls all of the programmed components. PSoC extends its computational capabilities by using mixed signal array, complex computations such as filtering, compression or suppression can be implemented at individual nodes. This affects in reduction of the data throughput over the network. Hence results in reduced transmission time and increased battery life of sensor node.

Thresholding Principle: Thresholding technique employed detects ECG signal accurately. Threshold value initially is set to low value which is 0.9mVolts typically. When ECG signal exceeds this value, R peaks are detected. Threshold value increases with time till the predefined high value of 1.32mVolts is reached. Threshold adaptive algorithm [11] is used to detect false beats and it automatically increases threshold value to increase noise immunity.

Heart rate classification: Based on the observed heart rate, ECG signal can be classified as bradycardia, normal or tachycardia. This allows transmitter to switch on transmit only if ECG is abnormal. Hence, saving power by large amount.

Rest of the paper is organized as follows. Section II review the related work carried in wireless ECG monitoring. Section III provides hardware and software platforms implemented. Section IV describes ECG detection, processing system using PSoC and Interface with CY3271 sensor node. Section V investigates the PSoC interfaced CY3271 sensor node. VI shows experimental results and analyses the improved system performance. Section VII concludes the paper and outlines future works.

II. RELATED WORK

Designs of ECG devices which are small in size, easy to wear, convenient to use and consume less power are being carried out very extensively. Advantages of WSN have made a popular choice among other techniques in designing such portable devices.

Ebrahim Nemati, M. Jamal Deen, and Tapas Mondal [6] have designed a small, portable two-lead capacitive coupling ECG sensor and a wireless module. This wireless module sends the processed ECG signal at patient side to a PC using the low power ANT protocol. Each node in an ANT network consists of an ANT engine and a host microcontroller unit (MCU). The ANT engine is responsible for establishing connection, maintaining connection and channel operation. However, the MCU handles the specifics of a particular application. Low power consumption is achieved by switching node on and off based on their neighbour's nodes activity. ANT network employs such intelligence to overcome high power consumption.

Ebrahim Nemati, M. Jamal Deen, and Tapas Mondal [7] have designed WSN using Zigbee protocol. System on Chip (SoC) provides low power solution to acquire ECG signal. Zigbee protocol uses 2.4 GHz transmitter and receiver. Transmitter and receiver use low noise amplifiers, differential power splitter (DPS), and quadrature mixer for low-IF architecture. These blocks provide good conversion gain and signal switching, making it ideal for use in low power applications.

Tsung-Heng Tsai, Jia-Hua Hong, Liang-Hung Wang, and Shuenn-Yuh Lee, [8] have designed a very low power system on chip. This can be configured as wireless sensor node for continuous and real time health monitoring. SoC transmits acquired ECG signal over 433.95 MHz channel. Transmitted signal can be received by personal server like PDA. On PDA ECG signal is displayed and monitored. SoC consumes 700 uWatt with 0.7 V supply. This can run more than 200 hours, without changing it. This makes it a low power WSN solution.

Fei Hu, Yang Xiao [9] have proposed WSN design based on RF mote and Cypress's Programmable System on Chip (PSoC). PSoC's complex computational capabilities process different medical signals. Wavelet based signal decomposition technique extracts feature parameters. Based on these parameters normal or abnormal signal classification is done. RF mote transmits only abnormal signals to base station, thereby reducing network traffic, data throughput and transmission time.

Fei Hu, Shruti Lakdawala, Qi Hao and Meikang Qiu have designed WSN, using PSoC and MICA2 (Crossbow Inc.)[10]. PSoC is used to detect ECG signal. PSoC facilitates low data transmission by transmitting only abnormal ECG signal. This reduces congestion and data traffic over network. Low data rate reduces burden on MICA2 mote, thereby reducing power consumption.

In the proposed work, entire system is carefully designed to optimize power consumption. Designed system detect ECG signal and transmit it efficiently to base station located at around 100 meters. PSoC is interfaced with CY3271 sensor node, which transmits heart rate to the base station Electric pulse detection is implemented using thresholding technique for accurate ECG signal detection. Peak detector is used to detect R peak. Based on duration of R-R interval heart rate is calculated. Sensor node observes the data and transmits if heart rate is found as abnormal. This technique lowers heart rate transmission and reduces overall transmission power consumption. Heart rate can be recorded using GUI for later analysis purpose.

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III. HARDWARE AND SOFTWARE PLATFORMS

This section deals with hardware and software implementation techniques of PSoC and sensor node.

A. PSoC Hardware Platform

Cypress Semiconductor's family of PSoC microcontrollers are designed to replace traditional microcontroller-based system components with one low-cost programmable device. PSoC architecture has a central processor, data SRAM, flash program memory, configurable analog and digital blocks, programmable I/O ports, clock generator, and some other system resources. The M8C microprocessor follows 8-bit Harvard architecture and can operate on speeds of up to 24 MHz. The general purpose I/O pins (GPIO) allow flexibility to interface with external devices. Each pin's drive mode can select to predefined settings and interrupt option generates an interrupt in case of predefined events on a pin.

PSoC CY8C27443 with 28 pin PDIP package is used in our design. It contains 12 Rail-to-Rail Analog PSoC Blocks with 14-Bit ADCs, 9-Bit DACs, PGA's, Programmable Filters and Comparators. It also contains 8 Digital PSoC Blocks with 8 to 32 Bit Timers, Counters, and PWMs and Full-Duplex UARTs. It has inbuilt 256 bytes of RAM and 16 KB of program memory. It works on supply voltage ranging from 3.0 V to 5.25 V.

B. Wireless Sensor Hardware and Software Platform

CY3271 sensor node sensor node consists of PSoC CY8C27443 and RF7936 transceiver. This is the application controller in node, where user application can be developed. It controls the RF 7936 Radio and other components on the board. To perform Input/output operation with external application board, Node application PSoC has five General Purpose Input Output pins (GPIO). Apart from these it also has two I2C pins Serial Data line (SDA) and serial clock (SCL).

Sensor node uses CyFi Star Network Protocol. Protocol stack is lightweight, occupies less than 6KB of code space for a node. This frees up more space for building the complete embedded wireless system in a single PSoC device. Sensor node can be operated by 2 AAA battery pack. CR-2032 coin cell battery pack can also power up sensor node.

C. PSoC Software Platform

The PSoC designer integrated development environment (IDE) is developed by Cypress Microsystems. PSoC Designer is the revolutionary IDE that can be used to customize PSoC to meet specific application requirements. PSoC Designer software accelerates system time to market. Applications can be developed using a library of pre characterized analog and digital peripherals in a drag and drop design style. Customized design leverage the dynamically generated API libraries of code. Finally we can debug and test developed designs with the integrated debug environment, including in-circuit emulation and standard software debug features.

The PSoC application code is developed in three main stages,

1) *Device editor (DE):* It allows the user to choose the functional component (e.g. ADC, filter, timer, counter, etc.) for each of the analog/digital blocks.

2) *Application editor (AE):* It allows the user to write the code either in C language or assembly language. The analog/digital blocks must be initialized in the code using the generated component libraries. It also gives access to the interrupt service routine.

3) *Debugger:* Debugging is the last step in the development process of PSoC. PSoC designer IDE provides an in-circuit-emulator, which allows debugging at the full operating speed of PSoC. It allows the user to define complex breakpoint events and large trace buffers that allow the user to monitor registers, memory locations, etc.

IV. ECG DETECTION AND PROCESSING SYSTEM USING PSOC AND INTERFACE WITH CY3271 SENSOR NODE

This section deals with interface design between PSoC and CyFi CY3271. This is achieved by implementing a Serial Peripheral Interface (SPI) in full duplex mode between them. SPI master implemented here transmits data to the slave at the clock speed specified on Serial Clock (SCLK). Slave select (~SS) line controls SPI slave i.e SPI slave reads data from its internal buffer after asserting ~SS signal. Clock rate must be set to two times the desired bit rate.

A. Programming PSoC to detect and transmit ECG signal

ECG signal first should be detected from sensor. After processing, heart rate should be sent on SPI Master Out Slave In (MOSI) line to the node PSoC for transmitting signal to the base station.

1) *Amplifier:* The programmable gain amplifier (PGA) is used to provide high input impedance to sensor connected to it. It amplifies the signal to the desired level based on the user requirement. It uses only one analog block for its operation. In our design, the PGA gain is set to 48. Reference is selected as a GND. Analog bus is disabled.

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Since gain is greater than one, top of the resistor string is connected to the Op Amp output and the resistor tap is connected to the inverting input of the Op-Amp.

2) *Analog to Digital Converter:* PSoC processes data in digital form. Thus analog data has to be converted into its digital form for this reason. For our design, a variable 14 bit resolution incremental ADC has been selected. This provides flexibility to finely tune the sample rate and change the resolution as per the application requirement during the development stage. It comprises of integrator, comparator, counter, pulse width modulator (PWM) and some reference signals. Data clock of 8MHz has been selected. This module use one analog block and four digital blocks for 8-bit counter and 24 bit PWM.

3) *SPI Master and Buffer:* This block performs full duplex synchronous 8-bit data transfers. SCLK phase, SCLK polarity, and LSB First options specify SPI clocking modes. SPI clock mode 0 is used in our design. Data clock is set as 93.75 KHz. This option selects data transfer rate. This block uses one digital block to accomplish its operation.

In order to drive the data on MOSI line of SPI slave, digital buffer is used. Clock should be synced with system clock to achieve proper operation. This block uses one digital block.

These 3 user modules are selected from user module available in design editor. They are configured using above values and routed.

B. Filter and Thresholding implementation in firmware

ECG signal gets corrupted from sources like electrical interference from surrounding equipment, measurement (or electrode contact) noise, electromyogram noise (muscle contraction), movement artifacts, instrument noise (such as artifacts from the ADC conversion). Thus ECG signal has to be filtered using digital filters.

1) *Second order IIR Low Pass Filter:* A cascade of three second-order IIR lowpass filters the ADC samples. In general, an IIR filter is represented by equation 1 in which the output signal at a given instant is obtained as a linear combination of I/O signal samples at earlier times. These filters are designed to suppress the 50 and 60-Hz interference. Each has the following transfer function with a cut-off frequency of 25 Hz.

$$H(z) = \frac{0.0625(1+Z-2)+0.125z-1}{1-0.75z-1+0.25z-2} \qquad (1)$$

2) *Differentiator:* The first-order IIR high-pass filter with a cut-off frequency (FC) of 70 Hz determines the first derivative of the ECG signal used for pulse rate calculations. This is represented by equation 2. The derivative picks out the QRS complex from the ECG signal.

$$H(z) = \frac{0.5(1-z-1)}{1-0.015625z-1} \qquad (2)$$

3) *Peak Detector:* A smart peak detector with automatic threshold adjustment is used to detect R-R peaks. R-R interval is measured. Heart rate is calculated by taking reciprocal of this mean pulse interval value over a fixed period of time of 60 sec and then scaling to units of beats per minute (BPM). This calculated heart rate is made pass through averaging filter. Filter calculates average of last two detected heart rates. This is done to improve accuracy of the system.

4) *Threshold adaptive algorithm:* Thresholding technique helps in detecting ECG signal. Threshold value increased from low level, till it reaches the desired high level. Whenever ECG signal crosses this threshold value, a QRS complex will be detected.

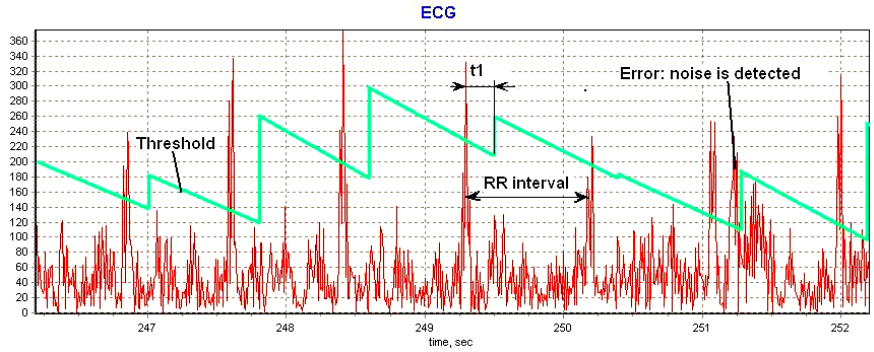

Fig. 2. Thresholding and noise detection

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To reduce the detection of false beats, after every detected QRS complex, the algorithm performs the automatic threshold level adjustment and noise detection in 240 msec, this is shown in Fig. 2.

Algorithm works as follows,

Step1-Find maximum absolute value in an interval of t1 = 200 msec after the last detected complex.

Step2 –Update threshold value with 0.75 × max [E], where E is the differentiated ECG.

Step3- Decrease threshold value till it reaches predefined value.

Step4- During interval between 200 msec to 240 msec following last QRS detection, if E becomes greater than threshold value then goto step 5. Else, goto Step1.

Step5- Display "noise" is detected. Increase threshold value, recount current R-R interval. Goto, Step1.

V. APPLICATIONS OF THE PSOC INTERFACED CY3271 SENSOR NODE

This section investigates working of CY3271 sensor node interfaced with PSoC.

A. CY3271 Programming

Heart rate sent by SPI master on MOSI line should be collected and stored for later transmission. Hence, a SPI Slave should be used for this purpose. CyFi Star Network Protocol (CYFISNP) user module is used to configure RF7936 transceiver.

1) *SPI Slave and buffer:* Implemented similar to SPI master. Proper care must be taken while interconnecting MOSI, MISO, SCLK and ~SS lines with that of master. External clock is not used as the data transfer takes place at the clock rate set by master. This module uses one digital block. Data sent to this node can be buffered back to PSoC after buffering. This module uses one digital block.

2) *CYFISNP:* This user module controls the operation of RF transceiver by calling CYFISNP API's. Node Power Supply Type is set as low impudence alkaline battery, which supplies continuous power to the node. Power consumption can be reduced using sleep timer. 255 bytes of EEPROM Block is selected to store network parameters. External Power Amplifier is used to conserve energy on the node. 6MHz data clock is used by SPI module to transfer/receive data to the node. Low RF channel 10 (2.412 GHz) and high channel 58 (2.460 GHz) to control RF emissions. This module use one digital block.

B. Abnormal heart rate detection

Sensor node receives data from PSoC. Following classification of ECG signal is used by the transmitter to make transmission decisions.

TABLE 1 HEART RATE CLASSIFICATION

Heart Rate	State
30-60BPM (default values, adjustable)	Bradycardia
60 -90 BPM (default values, adjustable)	Normal
90-120 BPM (default values, adjustable)	Tachycardia

C. Calculating R-R interval

To calculate power consumption by the transmitter, we need to calculate minimum and maximum heart rates that are transmitted per minute. R-R interval can be calculated using following formula,

R-R interval in seconds = 60sec/observed heart rate. (3)

When heart rate is normal, heart rate is never transmitted to the base station. If bradycardia or tachycardia is observed, it is abnormal heart rate. Transmitter will be switched on and transmits heart data of one byte.

Highest heart rate from Table 1 achieved is 120BPM. From equation 3, we can calculate R-R interval as 0.5 Seconds. Meaning, heart rate transmission happens every half a second.

D. Placing and routing in the DE:

CYFISNP and SPI Slave user modules are used to receive data from PSoC and transmit it over to base station. One bit is transmitted or received at two clock cycles. SPI Slave receives data from PSoC with clock rate set my master. Thus, receives data at 21.33µs, because SCLK on master is set as 93.75 KHz. CYFISNP is clocked at 6MHz. This module sends each bit over to radio module at 0.334µs speed.

E. Base station setup

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Base station is made up of a PC Bridge consisting of two CY8C28494 processors. One processor acts as the Master microprocessor that provides USB to I2C bridge functionality. The second CY8C28494 processor acts as the wireless hub and communicates with the Sense and Control Dashboard GUI via an I2C interface to the master processor USB/I2C bridge. The Wireless Hub application use the CyFiSNP user module configured as a hub to communicate with the wireless nodes. All configuration and node data between processors is communicated over a I2C interface. Hub configuration is provided with the kit. It must be downloaded into the hub to make it working as receiver.

Sense and control dashboard is used to bind the sensor node and configure it. Logged data at the node is received and displayed on this GUI. This GUI also provides flexibility of saving the data on PC for later analysis.

VI. RESULTS AND PERFORMANCE ANALYSIS

A. CY3271 sensor node performance result

Cypress Microsystems have designed a power calculator using simple excel sheet and is freely available for their users to calculate power. This helps developers to estimate the power consumption in the chip. Power consumption is calculated based on number of analog/digital peripheral blocks used, frequency of clock used for each of them, the number of pins and rows (on which the signals are routed) to be driven, etc. Fig. 3 shows power calculator result of sensor node. Sensor node operates on 3.3 V and use 6MHz for its internal operations. CYFISNP operates on 6MHz. Provides clock to radio on Row_0_Output_3 line at 6MHz and consumes 0.095mA of current. Similarly this module sends data to radio module on Row_0_Output_1 line at 6MHz, consuming 0.095mA of current. Data at node is sent back to PSoC on Row_1_Output_1, at 93.75 KHz speed consuming 0.008mA of power. MOSI, SS and SCLK data from master are received on GPIO lines at 9.75 KHz, consume 0.035mA. Overall power consumption including reference circuit current is calculated as 3.452mA.

Table 2 shows the comparison results between the implemented system (Model 2) and thresholding system (Model 1). Model 1 compares performance with MICA2 mote. Whereas, Model 2 compares performance with Model 1 and MICA2 mote. Three cases have been considered for performance comparisons.

1) *Case1:* 100% of the time ECG signal is below threshold. Model 1 never transmits the data. This is same case for Model 2, as heart rates are never transmitted to base station when normal heart rate is observed.

2) *Case 2:* 50% of the time ECG signal is below threshold. Model 1 sends three packets per second or 180 packets per minute. In Model 2, node transmits data when it detects heart rate as either bradycardia or tachycardia. Model 2 assumes tachycardia heart condition for analysis purpose, as highest heart rate is possible here. Thus for one minute maximum of 120BPM is considered. Then number of data transmission packets per minute is calculated as 120. For 50% below threshold, 60 packets per minute or one packet per second is transmitted.

3) *Case 3:* 0% of the time ECG signal is below threshold. Model 1 transmits 28 packets per second or 1680 packets per minute. Model 2 transmits 120 packets per minute or two packets per second. Detection technique employed in Model 2 reduces number of packets transmitted per minute by a large extent.

B. Sense and Control Dashboard

SCD facilitates doctors by storing individual patient's data on PC. This helps to carry out further clinical research. Fig. 4 shows data logging of patient with heart rate of 60BPM. It can be observed that 60 packets get received per minute. Meaning, one packet per second. Message and time stamp fields in Fig. 4 indicate, base station receives heart rates at various time instance.

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Estimated PSoC Power Calculations for CY8C27xxx Family Device											
Version 1.0									Enter parameters in yellow		
project name	CY 3271 Sensor Node								See estimated result in green		
part number	CY8C27443			**Cypress MicroSystems, Inc.**					Indicates something is wrong		
pin count	28										
								OpAmp Bias	0		
CPU Clock	12.000	MHz		SysClkx2Disable	1						
Vdd	3.30	V							Power		
								Analog Block	Level (0-3)		
CPU Current	2.764	mA						ACB00	0	0.000	mA
								ACB01	0	0.000	mA
								ACB02	0	0.000	mA
	Block Clk			GPIO	GPIO Clk			ACB03	0	0.000	mA
Digital Block	(MHz)			Count	(MHz)			ASC10	0	0.000	mA
DBB00	0.032	0.005	mA	3	0.094	0.034	mA	ASD11	0	0.000	mA
DBB01	0.000	0.000	mA	0	0.000	0.000	mA	ASC12	0	0.000	mA
DCB02	6.000	0.066	mA	0	0.000	0.000	mA	ASD13	0	0.000	mA
DCB03	0.000	0.000	mA	0	0.000	0.000	mA	ASD20	0	0.000	mA
DBB10	0.000	0.000	mA	0	0.000	0.000	mA	ASC21	0	0.000	mA
DBB11	0.000	0.000	mA	0	0.000	0.000	mA	ASD22	0	0.000	mA
DCB12	0.000	0.000	mA	0	0.000	0.000	mA	ASC23	0	0.000	mA
DCB13	0.000	0.000	mA	0	0.000	0.000	mA	Analog Block Current		0.000	mA
Digital Block Current		0.071	mA	GPIO Current		0.034	mA				
								A_Buffer Power	0		
	Row Clk			Analog Power				Analog			
Row	(MHz)			All Off	0			Output Buffer			
Row_0_Output_0	0.000	0.000	mA	SC Off/Ref Low	0	0.000	mA	AnalogOutBuf_0	0	0.000	mA
Row_0_Output_1	6.000	0.095	mA	SC Off/Ref Med	0	0.000	mA	AnalogOutBuf_1	0	0.000	mA
Row_0_Output_2	0.000	0.000	mA	SC Off/Ref High	0	0.000	mA	AnalogOutBuf_2	0	0.000	mA
Row_0_Output_3	6.000	0.095	mA	SC On/Ref Low	1	0.385	mA	AnalogOutBuf_3	0	0.000	mA
Row_1_Output_0	0.000	0.000	mA	SC On/Ref Med	0	0.000	mA	Analog Output Buffer Current		0.000	mA
Row_1_Output_1	0.094	0.008	mA	SC On/Ref High	0	0.000	mA				
Row_1_Output_2	0.000	0.000	mA	Reference Circuit Current		0.385	mA	**Estimated Total PSoC Current**		**3.452**	**mA**
Row_1_Output_3	0.000	0.000	mA								
Row Current		0.198	mA					**Estimated Total PSoC Power**		**11.393**	**mW**

Fig. 3 Power consumption of application PSoC in intelligent sensor node.

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TABLE 2 PERFORMANCE EVALUATIONS OF SENSOR NODES SYSTEMS, WITH PSOC INTERFACE

CASE I: 100% of the time below threshold							
	Mica 2 Mote	**Model 1**			**Model 2**		
Radio		**% Current Consumed**	**% Current Reduced**	**Observed Value**	**% Current Consumed**	**% Current Reduced**	**Observed Value**
Current Transmit in mA	12	8%	92%	0.96	8%	92%	1
Current Receive in mA	8	0%	0%	--	0%	0%	--
Current Sleep in mA	0.002	92%	8%	0.0018	83%	18%	0.0016
PSoC							
Active Current in mA	3.774	100%	0%	3.774	91%	9%	3.452
Current Consumption in mA	23.7740	20%	80%	4.7358	19%	81%	4.4536
% Current Consumption Reduced by Model 2 over Model 1:		5.96%					
CASE II: 50% of the time below threshold							
	Mica 2 Mote	**Model 1**			**Model 2**		
Radio		**% Current Consumed**	**% Current Reduced**	**Observed Value**	**% Current Consumed**	**% Current Reduced**	**Observed Value**
Current Transmit in mA	12	44%	56%	5.28	37%	63%	4.45
Current Receive in mA	8	0%	0%	--	0%	0%	--
Current Sleep in mA	0.002	56%	44%	0.00112	54%	46%	0.001
PSoC							
Active Current in mA	3.774	100%	0%	3.774	91%	9%	3.452
Current Consumption in mA	23.7740	38%	62%	9.05512	33%	68%	7.903
% Current Consumption Reduced by Model 2 over Model 1:		12.72%					
CASE III: 0% of the time below threshold							
	Mica 2 Mote	**Model 1**			**Model 2**		
Radio		**% Current Consumed**	**% Current Reduced**	**Observed Value**	**% Current Consumed**	**% Current Reduced**	**Observed Value**
Current Transmit in mA	12	80%	20%	9.6	74%	26%	8.9
Current Receive in mA	8	0%	0%	--	0%	0%	--
Current Sleep in µA	0.002	20%	80%	0.0004	17%	83%	0.0003
PSoC							
Active Current in mA	3.774	100%	0%	3.774	91%	9%	3.452
Current Consumption in mA	23.7740	56%	44%	13.3744	52%	48%	12.3523
% Current Consumption Reduced by Model 2 over Model 1:		7.64%					

Hub VendorID	**Hub ProductID**	**HubSerialN**	**NodeID**	**Resp**	**Rem**	**Len**	**RSSI**	**Time Stamp**	**Message In Hex**
0x04B4	0xF115	8819DDC34222	01	00	00	01	10	04:09:04	46
0x04B4	0xF115	8819DDC34222	01	00	00	01	11	04:09:05	46
0x04B4	0xF115	8819DDC34222	01	00	00	01	11	04:09:06	46
0x04B4	0xF115	8819DDC34222	01	00	00	01	0F	04:09:07	46
0x04B4	0xF115	8819DDC34222	01	00	00	01	10	04:09:08	46
0x04B4	0xF115	8819DDC34222	01	00	00	01	13	04:09:09	46
0x04B4	0xF115	8819DDC34222	01	00	00	01	10	04:09:10	46
0x04B4	0xF115	8819DDC34222	01	00	00	01	13	04:09:11	46
0x04B4	0xF115	8819DDC34222	01	00	00	01	15	04:09:12	46
0x04B4	0xF115	8819DDC34222	01	00	00	01	10	04:09:13	46

Fig. 4 Data logging by sensor node with NodeID 1

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VII.CONCLUSION AND FUTURE WORK

This work implements low power design by interfacing PSoC with CY3271 sensor node. ECG detection and processing system demonstrates its ability to detect ECG signal. Threshold adaptive algorithm was developed to facilitate accurate ECG detection. Heart rate classification is done in sensor node and its performance is analyzed. It was observed that in comparison with thresholding technique employed by PSoC interfaced MICA2, electrical pulse detection method employed in this work decreases number of packets transmitted per second. Intelligent sensor node enables transmission only when critical heart event is detected. Observations showed that, the node PSoC's current consumption was less than that of MICA2. Reduced data packet and intelligence of sensor node contributes in reduction of overall systems current consumption. This will lead to reduction of data traffic at individual nodes on sensor network and improves lifetime of sensor node. ECG data logging on SCD by individual nodes help in analyzing the data for later use.

CY3271 is strong enough to handle radio as well as node application PSoC. Since network protocol stack uses code less than 6Kbytes, entire ECG detection and wireless transmission system application can be developed on CY3271. PSoC used in detection system and sensor node consume about 9.5mA and 3.452mA respectively. Require individual battery to power up. Complete application designed on CY3271 should curtail current consumption and cost. Small size, light weight, low power consumption and ability to perform complex computations make PSoC one of the best choices in developing medical applications.

REFERENCES

[1] **I. F. Akyildiz, W. Su, Y. Sankarasubramaniam, and E. Cayirci**, "Wireless sensor networks: A survey", Computer Networks (Elsevier) Journal, pp. 393-422, 2002.

[2] **N. A. Khan, N. Javaid, Z. A. Khan, M. Jaffar, U. Rafiq, A. Bibi ,** "Ubiquitous HealthCare in Wireless Body Area Networks", IEEE 11th International Conference on TrustCom, pp.1960-67, 2012.

[3] **Fred Chen, Henry Wu, Pei-Lan Hsu, Brad Stronger, Robert Sheridan, and Hongshen Ma,** "SmartPad: A Wireless, Adhesive-Electrode-Free, Autonomous ECG Acquisition System*",* EMBS, 30th Annual International Conference of the IEEE, pp. 2345-48, 2008.

[4] **Chulsung Park and Pai H. Chou, Ying Bai, Robert Matthews, and Andrew Hibbs**, "An Ultra-Wearable, Wireless, Low Power ECG Monitoring System", Biomedical Circuits and Systems Conference of the IEEE, pp. 241-44, 2006.

[5] **Massot B, Gehin C, Nocua R, Dittmar A, McAdams E**,"A wearable, low-power, health-monitoring instrumentation based on a Programmable System-on-Chip", EMBC, Annual International Conference of the IEEE, pp. 4852-55, 2009.

[6] **Ebrahim Nemati, M. Jamal Deen, and Tapas Mondal,** "A Wireless Wearable ECG Sensor for Long-Term Applications", Communications Magazine, IEEE, Vol.50 (1), pp. 36-43, 2012.

[7] **Tsung-Heng Tsai, Jia-Hua Hong, Liang-Hung Wang, and Shuenn-Yuh Lee**, "Low Power Analog Integrated Circuits for Wireless ECG Acquisition Systems", Information Technology in Biomedicine, IEEE Transactions, Vol. 16 (5), pp. 907-917, 2012.

[8] **Tee Hui Teo, Xinbo Qian, Pradeep Kumar Gopalakrishnan, Yee Shan Hwan, Kuruveettil Haridas, Chin Yann Pang, Hyouk-Kyu Cha, Minkyu Je**, "A 700-µW Wireless Sensor Node SoC for Continuous Real-Time Health Monitoring*",* Solid-State Circuits, IEEE Journal Vol. 45 (1), pp. 2292-99, 2010.

[9] **Fei Hu, Yang Xiao**, "Congestion-Aware, Loss-Resilient Bio-Monitoring Sensor Networking for Mobile Health Applications", Selected Areas in Communications, IEEE Journal Vol.27 (4), pp. 450-465, 2009.

[10] **Fei Hu, Shruti Lakdawala, Qi Hao and Meikang Qiu,** "Low-Power, Intelligent Sensor Hardware Interface for Medical Data Preprocessing*",* Information Technology in Biomedicine, IEEE Transactions, Vol.13 (4), pp. 656-63, 2009.

[11] **Serhiy Matviyenko**, Cypress application note *AN2284*, "Low Cost EKG Pulsometer", Document no. 001-25719, 2006.

[12] **Archana Yarlagadda**, Applications Engineer, Cypress Semiconductor Corp "Designing a Wireless Heart Rate Monitor with Remote Data Logging", 2009. [Online] Available: *http://www.wirelessdesignmag.com.*

[13] (2008), The CY3271 sensor node website. [Online]. Available: *http://www.cypress.com/CY 3271 sensor node*.

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