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Reduction of Standby Leakage Power in CMOS VLSI Systems

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ABSTRACT: In this paper, a novel low-power design technique is proposed to minimize the standby leakage power in CMOS very large scale integration (VLSI) systems by generating the adaptive optimal reverse body-bias voltage.
In order to minimize the leakage power dissipation, several circuit techniques have been proposed, such as multi-threshold voltage CMOS (MTCMOS) and variable threshold voltage CMOS (VTCMOS) using variable substrate bias voltage. The adaptive optimal body-bias voltage is generated from the proposed leakage monitoring circuit, which compares the sub threshold current (ISUB) and the band-to-band tunnelling current (IBTBT). The proposed circuit was simulated in MICROWIND using a 32-nm bulk CMOS technology and evaluated further. The proposed approach demonstrates that the optimal body bias reduces a considerable amount of standby leakage power dissipation in CMOS integrated circuits. In this approach, the temperature and supply voltage variations are compensated by the proposed feedback loop.

KEYWORDS: Band-to-band tunnelling (BTBT) leakage, gate leakage, leakage current, leakage power, optimal body bias volt-age, sub threshold leakage.

I.INTRODUCTION

One of the primary objectives of cognitive radio (CR) over the past four decades, the size of transistors has continuously been reduced during the process of manufacturing to increase the device speed, density on a given chip, and the die yield. For device reliability and constant power dissipation per unit area, the supply voltage has been reduced as well. Therefore, continuous reduction in the threshold voltage of the transistor ensured high drive current. Hence, performance improvement is inevitable. Recently, as the supply voltage approaches 1V, conventional scaling has deviated from ideal constant-field scaling due to the difficulty of further lowering the threshold voltage (Vth).
This fundamental problem stems from the non-scalable characteristic of the thermal voltage (VT = kT/q), which causes relatively fixed sub threshold swing (S) at a constant temperature. This, in turn, increased the sub threshold leakage of current exponentially as the V_{th} value reduces. Therefore, there exists a lowest possible value of Vth, which is determined by the application constraints related to power consumption and circuit functionality.
In particular, for high-performance (HP) logic technology, certain level of overdrive voltage (VDD − Vth) should be maintained. This determines the drive current and hence the performance in a chip.

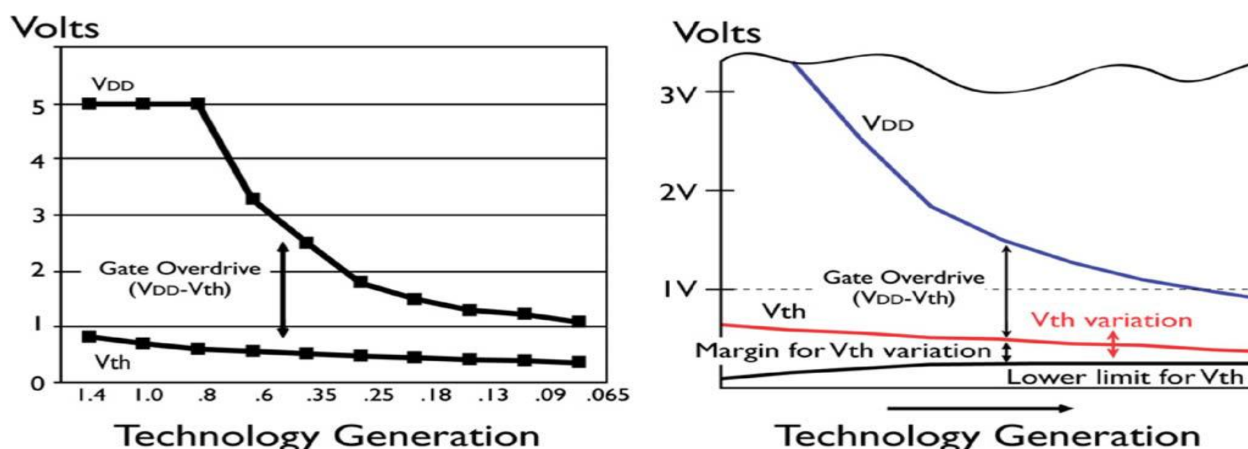

Figure 1: Trend of supply voltage and threshold voltage.

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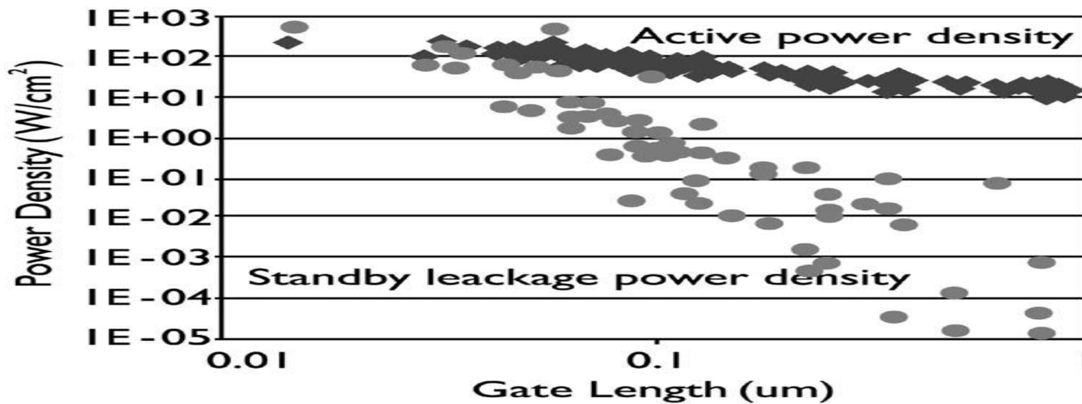

Figure 2: Power density trends for the active power and the standby leakage.

This situation makes it difficult to accomplish the further supply voltage scaling. Figure 1 shows the difficulty of further supply voltage scaling. Under fixed V^{th}, the reduction of VDD trades off performance (speed) and leakage power. Figure 2 shows the power density trends for active and standby leakage power with respect to different channel lengths.

Among the leakage power reduction techniques, the reverse body biasing (RBB) technique, which increases the threshold voltage (V^{th}) of transistors during standby mode, has widely been employed to suppress the sub threshold leakage Current (ISUB). However, this technique also aggravates short channel effects (SCEs), such as drain-induced barrier lowering (DIBL),

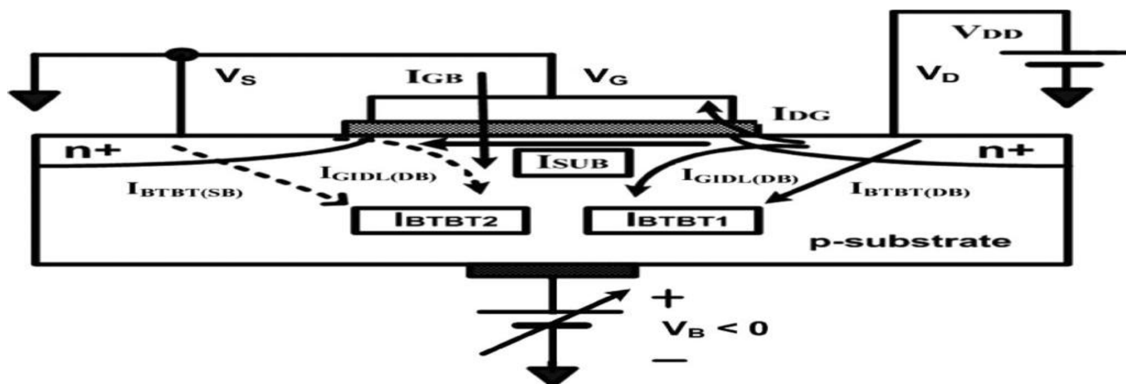

Figure 3: Standby leakage current components under reverse body bias (rbb).

Channel materials, etc. Furthermore, the reduction of the gate oxide thickness causes a drastic increase in tunnelling through the gate oxide. This is a strong exponential function of the voltage magnitude across the gate oxide. Consequently, to minimize the leakage power in standby mode, those leakage components have to be taken into account when the RBB technique is used.

The adaptive RBB technique has been proposed in this paper. However, the previous techniques require significant circuit modification and performance overhead for leakage reduction. Those techniques have not been complete or robust enough to apply to very large scale integration (VLSI) systems. This is because all the leakage-current components and minimum supply voltage are not considered for leakage power reduction. While it shows that the leakage power can significantly be decreased using both optimum power supply voltage and optimal body bias voltage, it requires a lot of circuit overhead. Therefore, this paper proposes a new standby leakage power reduction technique applicable to VLSI systems by exploiting the body bias voltage scaling only while all the other leakage currents are taken into account. The proposed approach significantly reduces the required hardware compared with by optimizing the body bias voltage only at the cost of efficiency of the standby current minimization.

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II. STANDBY LEAKAGE CURRENT COMPONENTS IN MOSFET UNDER RBB (REVERSE BODY BIAS)

CR-Networks Fig. 3 shows the leakage current ($I_{leakage)}$ components under the reverse body-bias condition. The total leakage current in the OFF-state n-MOSFET is given by

$$I_{leakage} = I_{SUB} + I_{BTBT}(DB) + I_{BTBT}(SB) + I_{GIDL}(DB) + I_{GIDL}(SB) + I_{GB} + I_{DG} \quad (1)$$

Where ISUB is the sub threshold leakage current, IBTBT(DB) and IBTBT(SB) are the BTBT leakage currents (drain-to-bulk and source-to-bulk reverse-bias p-n junction leakage currents),IGIDL(DB) and IGIDL (SB) are the GIDL currents, IGB is gate-to-bulk oxide tunnelling leakage current, and IDG is drain-to-gate oxide tunneling leakage current.

The sub threshold leakage current is the weak inversion conduction current dominated by the diffusion current flowing between the drain and the source when |VGS| < |Vth |. This Weak inversion conduction current is given by

$$I_{sub}=\mu CdepW/LV^2T \ [exp \ (VGS-Vth/nVt)) \ (1-exp \ (-VDS/Vt)] \quad (2)$$

(SAF where Cdep = εsiqNsub/(4φB) denotes the capacitance of the depletion region under the gate area, εsi is the permittivity of Si, q is the electron charge, Nsub is the doping concentration of the p-substrate, φB is the built-in potential, VT is the thermal voltage that is equal to kT /q, Cox is the oxide capacitance per unit area between the gate metal and the bulk surface, and n is the sub threshold parameter and is expressed as 1 + Cdep/Cox.

As shown in (2), when the MOSFET is off (VGS =0 V), the sub threshold current exponentially increases with the decrease of the threshold voltage. On the other hand, the tran-sistor threshold voltage equation considering the body effect is given by

$$V_{th}=V_{tho}+ \gamma(\sqrt{|2\Phi F +VSB/}-\sqrt{|2\Phi F|}) \quad (3)$$

where γ = is the body-effect coefficient, ΦF is the Fermi potential and is equal to (kT /q) ln(Nsub/ni), where ni is the intrinsic electron concentration, and VSB is the source-to-bulk potential difference. Since the sub threshold leakage current (ISUB) is the major leakage component, the RBB technique is used in this paper to reduce the total leakage current in standby-mode CMOS circuits by increasing the transistor threshold voltage. However, it is important to watch how other leakage current components change when the RBB is used to estimate the total leakage.

The BTBT leakage current, which is also called reverse-bias p-n junction leakage currents, is the current flow between the source/drain (S/D) and the substrate through the parasitic reverse-biased p-n junction diode during the OFF-state MOSFET. Once both S/D and substrate regions are heavily doped, then BTBT significantly increases. This is because the electric field across the junction depletion region increases. If the high electric field (> 106 V/cm) is formed across the reverse-biased junctions of the source/drain (S/D) regions, then a significant amount of BTBT current flows through the S/D to the substrate junctions. This is due to the voltage drop across the junction that is bigger than the band gap of silicon, particularly with increasing S/D voltage or reverse body bias. In Nano meter devices, higher channel and S/D doping with shallow junction depths are required to minimize SCEs, which cause a significant increase in BTBT current.

The GIDL current, which is also called as the surface BTBT current, causes the drain-to-substrate leakage due to the BTBT current in very high field depletion region, especially in the gate-drain overlap region. When the drain of an n-MOSFET is biased at the supply voltage (VDD) and the gate is biased at either zero or negative voltage, a depletion region is formed under the gate and drain overlap region. Similar to the BTBT current, if the high electric field is formed in the narrower depletion region as a result of the reverse bias between channel and drain, then a significant amount of surface BTBT current flows through the drain-to-substrate junctions due to the twisting of band gaps. With higher supply of voltage, thinner oxide thickness, lightly doped drain, reverse body bias (RBB) technique, and high mobility channel materials having smaller band gaps, the GIDL current is enhanced. IGB refers to the gate-to-bulk oxide tunnelling leakage current, and IDG refers to the drain-to-gate oxide tunnelling leakage current. As the gate oxide thickness scales below 2 nm, the direct tunnelling (DT) gate leakage exponentially increases due to quantum mechanical tunnelling. The DT gate leakage current not only increases the standby power dissipation but also limit the proper logic gate operation. Recently, a high-k dielectric base on Hafnium and dual metal gate has been introduced to

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increase the transistor performance. The high-k dielectric material reduces the gate leakage as the gate dielectric thickness can actually be increased while the gate capacitance is increased.

III. OPTIMAL BODY-BIAS VOLTAGE AND SUPPLY VOLTAGE

As explained in the previous section, the main components of standby leakage power are the gate tunneling leakage power, the sub threshold leakage power, and the reverse biased junction BTBT leakage power. For convenience, let us denote that

$I_{BTBT1} = I_{GIDL}(DB) + I_{BTBT}(DB)$, $I_{BTBT2} = I_{GIDL}(SB) + I_{BTBT}(SB)$, Igate = $I_{GB} + I_{DG}$, and $I_{BTBT} = I_{BTBT1} + I_{BTBT2}$.

Therefore, the total standby leakage power is given by

$$P_{leakage} \approx I_{gate}V_{gate} + I_{SUB}V_{SUB} + I_{BTBT}V_{BTBT} \quad (4)$$

Where V_{gate}, V_{SUB}, and V_{BTBT} are the voltage sources of each leakage component. The effect of body bias voltage and supply voltage on the standby leakage current for a 32 nm n-MOSFET Berkeley Predictive Technology Model has been reported. The gate leakage current is not significantly affected by V_{Body} since IDG is not function of V_{Body}. However, it exponentially increases with the increase of the supply voltage. As the supply voltage decreases from 0.9 to 0.5 V and the body bias voltage (V_{Body}) decreases from 0 to −2.5 V, the sub threshold leakage current decreases while the BTBT leakage current increases. As shown in (2), the sub threshold leakage current is an exponential function of the threshold voltage (V_{th}). Therefore, the RBB technique is an effective way to increase the threshold voltage (V_{th}) to suppress the sub threshold leakage current (I_{SUB}) in standby-mode CMOS circuits.

With the increase of reverse body bias, VSB becomes more positive, which results in higher threshold voltage and hence exponential decrease of the sub threshold current, as explained in (2) and (3). The plot of $I_{BTBT} + I_{SUB}$ explains why the leakage power consumption of a chip does not continue to monotonically decrease with increasing reverse body bias. At around −0.8 to −2.2 value of body bias voltage, the leakage power increases due to the highly increased I_{BTBT}. I_{gate} has less effect on the power variation. As a result, there is an optimal reverse body bias point that makes the minimal total standby leakage power of a device for each different supply voltage.

Therefore, the optimal body bias voltage that reduces the total leakage current is determined by the relationship between I_{SUB} and I_{BTBT}. In [6], I_{SUB} and I_{BTBT} are given in simplified form as follows:

$$I_{SUB} \approx ASeBSV_{Body} \quad (5)$$

$$I_{BTBT} \approx Abe{-}BbV_{Body} \quad (6)$$

where Ab, Bb, AS, and BS are the technology-dependent constants and V_{Body} is the body bias voltage.

The minimal leakage power with respect to an optimal VBody is calculated by the following equation:

$$\partial_{Pleakage} / \partial V_{Body} = 0 \quad (7)$$

Note that I_{gate} is ignored because the gate tunneling leakage changes little as V_{Body}.From the condition for minimal leakage power is obtained as follows:

$$B_{SISUB} = B_{bIBTBT} \quad (8)$$

The ratio of Bb and BS for the minimal leakage current determines the ratio of ISUB and IBTBT, as given in (8). Under the assumption of Bb/BS = 1, ISUB must be equal to IBTBT to reduce the leakage power. The optimal V_{Body} to reduce the sum of ISUB and IBTBT is found and it is smaller than V_{Body} to make ISUB equal to IBTBT. However, near the value of −1 V of V_{Body}, the total leakage current ($I_{SUB} + I_{BTBT} + I_{gate}$) is almost equal to I_{gate} i.e., V_{Body} that makes I_{SUB} equal to I_{BTBT} can be selected as a near-optimal value.

The significant leakage component, when the body-bias voltage is at the optimal value of V_{Body}, is the gate leakage I_{gate}. Therefore, the supply voltage must be decreased as much as possible to reduce I_{gate}. The reduction of supply voltage decreases the optimal reverse V_{Body}.

IV. CIRCUIT IMPLEMENTATION

4.1. Sub threshold Leakage Current Suppression Using Stack Effect:

The sub threshold leakage current is reduced when there are two or more stacked off-transistors. By turning off more than one transistor in a stack of transistors, it forces the intermediate node voltage to have a value higher than zero.

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This causes a negative VGS, VBS (more body effect), and VDS reduction (less DIBL) in the top transistor, thereby helping reducing the sub threshold leakage current flowing through the stack considerably. This is known as the stack effect, and these results in reduced sub threshold value of leakage current.

4.2. Proposed V_{Body} Control System:

In the previous section, the optimal V_{Body} points are found theoretically and through simulations/measurements of a MOSFET. In this section, the hardware implementation of the proposed V_{Body} control system that minimizes the overall power dissipation is introduced. This hardware allows the independent and adaptive adjustment and maintenance of the body-bias voltages when the operating conditions change. The proposed scheme in Fig. 4 consists of the leakage monitoring circuit, the current comparator, and the charge pump.

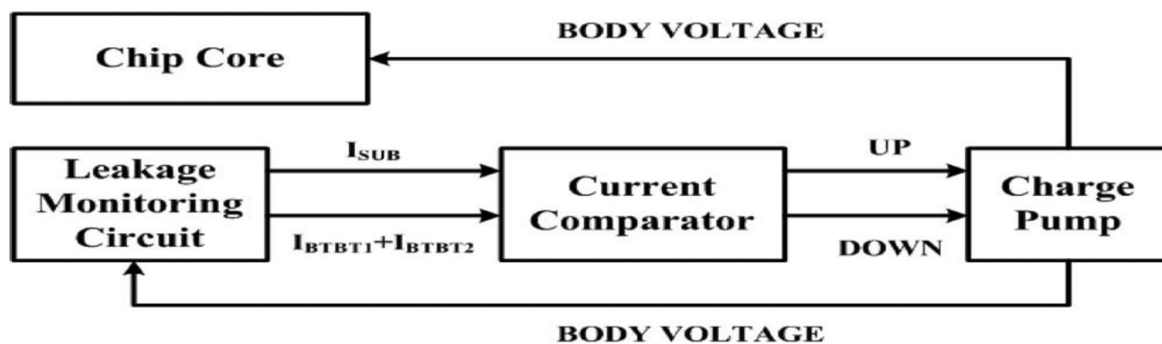

Figure 4: Block diagram of the proposed V_{Body} control system.

In the proposed scheme, a current comparator is used to determine the optimal body bias voltage target assuming the power supply is regulated outside the chip. The body bias voltages for n-MOSFET and p-MOSFET are automatically set by the control system to ensure that the chip dissipates minimal power in standby mode.

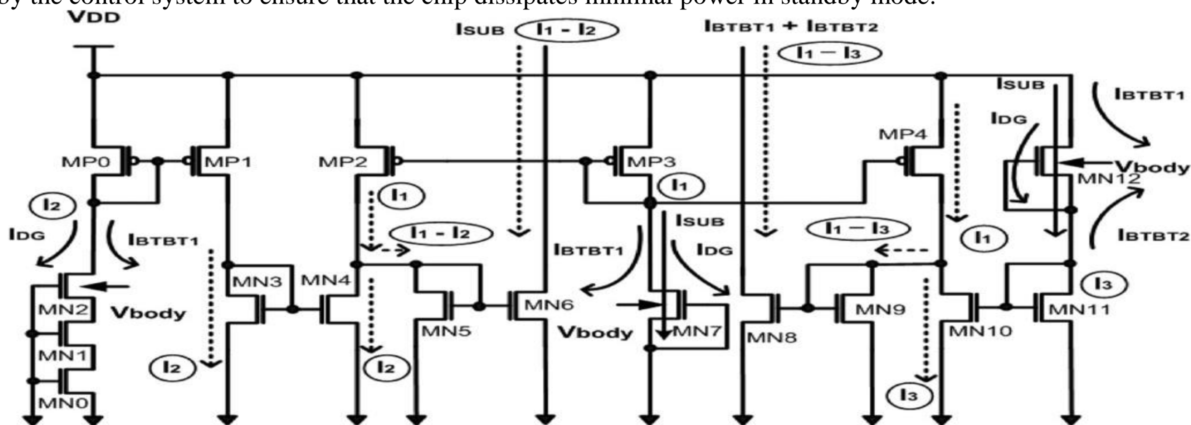

Figure 5: Leakage monitoring circuit for n-MOSFETs.

The proposed scheme uses the current mode circuit technique to process the active signals in the current domain, and it offers a number of advantages, such as better sensitivity, high speed, and low-power dissipation.

Since the circuits used in the proposed scheme are fully analog circuits, and the feedback loop continuously works, no control circuits are required. This is one of the main advantages of the proposed approach. The leakage monitoring circuit separates the sub threshold leakage (I_{SUB}) and the BTBT leakage current (I_{BTBT}1, 2) from the total leakage components. Fig. 5 shows a new leakage monitoring circuit for n-MOSFETs, where the transistors of MN2, MN7, and MN12 are the replica transistors to generate leakage components, and MP0/MP1, MP2/MP3, and MN10/MN11 form current mirrors. By using triple off-transistors in a stack, the sub threshold current flowing from drain to source of the MN2 transistor can be ignored. Therefore, the amount of drain current of the MN2 transistor denoted as I2 is approximately the same as the sum of I_{DG} and I_{BTBT1}.

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The drain current of MN7, which is denoted as I1, consists of I_{DG}, I_{BTBT1}, and I_{SUB}. In the source of the MN12 transistor, the current $I3$ consisting of I_{DG}, I_{BTBT2}, and I_{SUB} is generated. The leakage monitoring circuit for p-MOSFETs is made up with the same structure as the monitoring circuit for n-MOSFETs. Two current differential amplifiers are employed based on the generated leakage components. ISUB (current $I1$–current $I2$) is obtained through MN4, MN5, and MN6 transistors, whereas $I_{BTBT} = I_{BTBT1} + I_{BTBT2}$ (current $I1$–current $I3$) is obtained through MN8, MN9, and MN10 transistors.

The separated leakage components are applied to the current comparator to generate a pulse width proportional to the magnitude of each leakage. The current comparator is designed using the current mirrors, as shown in Fig. 6, where MN6 and MN8 in the monitoring circuit are connected to the current comparator. The current comparator offers good leakage

(Figure 5). Body bias voltage is generated in the optimal body bias voltage controller. Sensitivity, high speed, and low-power dissipation is the characteristics of such system. In Fig. 6, the comparator compares a current $I1$ and a current $I3$ with a current $I2$ and a current $I4$, respectively: $I1$ and $I4$ are generated

by I_{BTBT}, and $I2$ and $I3$ are generated by ISUB. There are three modes of operation of the current comparator.

1) If $I_{BTBT} = I_{SUB}$, $I1 = I2$, and $I3 = I4$, then $I5 = I6 = 0$, maintaining the body-bias voltage.
2) If $I_{BTBT} > I_{SUB}$ and $I1 > I2$, then $I6 > 0$, charging the output capacitor of the charge pump and increasing the body bias voltage.
3) If $I_{BTBT} < I_{SUB}$ and $I3 > I4$, then $I5 > 0$, discharging the output capacitor of the charge pump and decreasing the body bias voltage.

The charge pump discharges or charges its output capacitor, depending on two signals from the current comparator and its own bias voltage. The final output stage consists of an op-amp and a buffer. The current comparator-based circuit provides the optimal body bias voltage to match the sub threshold leakage with the BTBT leakage currents. The body-bias voltages for n-MOSFETs or p-MOSFETs are changed to the optimal body points within 10 ns, as shown in Fig. 10. In this paper, we concentrate on the N-MOSFET leakage current minimization based on an N-well P-type substrate process.

If the process is a P-well N-type substrate process, then the circuits that generate the optimum body bias voltage is complementary of the circuits shown in Figs. 4 and 6. The range of the body biasing voltage in this paper is between −0.9 and 0 V, and the sign of the V_{Body} is easily inverted before V_{Body} is applied to the substrate. Therefore, VDD and VSS are same for the whole system in this case.

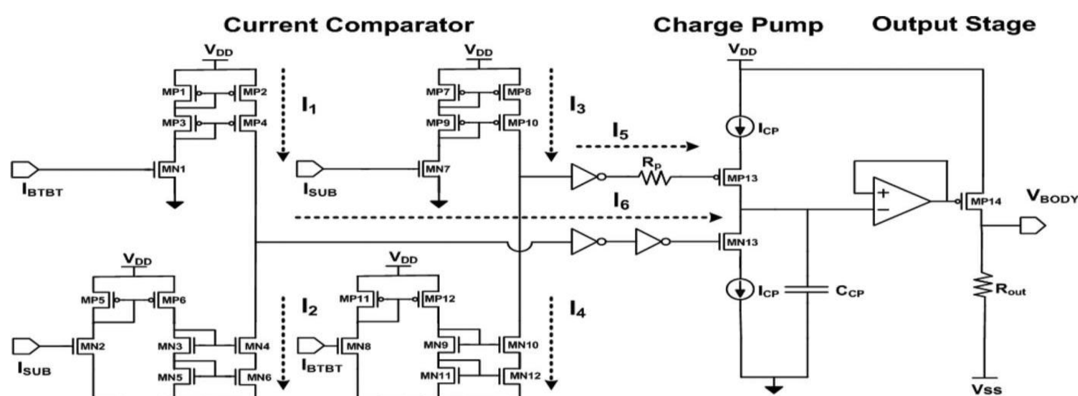

Figure 6: Schematic of the proposed V_{Body} control system.

VI.CONCLUSION

As the technology scaling goes down below 90 nm, the standby leakage power dissipation has become a critical issue. Therefore, the new circuit design technique for minimizing the leakage power must be developed along with the device scaling. To reduce the standby leakage power, this paper has presented a novel design technique that generates the optimal V_{Body} scaling during standby mode. By monitoring the band to band tunnelling current (I_{BTBT}) and the sub threshold leakage current (I_{SUB}), the optimal body-bias voltage is automatically generated and continuously adjusted by the control loop. By tuning the body bias voltage using the leakage-monitoring circuit, the circuit can be biased at the

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optimal point where the sub threshold leakage current and the BTBT leakage current are balanced to accomplish the minimum leakage power.

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