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Power Amplifier Linearization Using Multi-Stage Digital Predistortion Based On Indirect Learning Architecture

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ABSTRACT: Power amplifiers (PA) are one of the essential components of communication systems and are nonlinear in nature. The nonlinearity creates in band and out of band distortions. To linearize a PA the cost effective method is use of digital predistortion. In this paper we propose a multi stage algorithm for digital predistortion using QR Decomposition. The coefficients are estimated using Indirect Learning Approach (ILA). In multi stage ILA the predistortion is implemented in two or more stages as compared to the single stage implementation of the conventional ILA approach. The multistage predistorters can achieve the same performance or even better performance than single stage predistorter depending on the power amplifier with lower complexity. The complexity is measured by the number of coefficients required for the identification of the predistorter. The performance of the multistage ILA is evaluated in terms of improvement in spectral regrowth suppression when an OFDM signal is given as input signal. Wiener-Hammerstein model is used for PA modelling.

KEYWORDS: Power amplifiers; Digital predistortion; Wiener-Hammerstein model; Indirect Learning Approach (ILA); Least Squares method; QR Decomposition.

I. INTRODUCTION

Power amplifiers are one of the essential components of a communication system and are inherently nonlinear in nature. This nonlinear nature produces in-band distortion (BER performance deterioration) and out-of-band distortion (Spectral regrowth beyond signal bandwidth) [1, 2]. For low power amplifiers and narrow band input signals, the power amplifiers can be modelled as memoryless nonlinearity [3]. In memoryless PA the current output of PA depends only on current input to PA. With the use of wideband signals such as OFDM or WCDMA in communications the power amplifier tend to exhibit memory effects. The memory effects arise due to the presence of thermal constants of active devices which are having frequency dependent behaviours. Now the current output of PA not only depends on current input to PA but also the past input values to PA. The memory effects further deteriorate the transmitted signals resulting in more out-of-band and in-band distortions.

Various methods have proposed for the linearization of power amplifiers so as to increase the efficiency such as feedforward linearization [4], feedback linearization [5], predistortion [6] etc. Out of all methods available the Digital predistortion [6] (DPD) is the most cost effective method for linearization of PA. In baseband digital predistortion, basically we place a predistorter block just before the power amplifier which is having the inverse nonlinear characteristics

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of that of PA (see Fig.1.1). Thus the cascaded predistorter-PA system can work as a linear system and PA can be driven more to the high efficiency saturation region without compromising much on linearity.

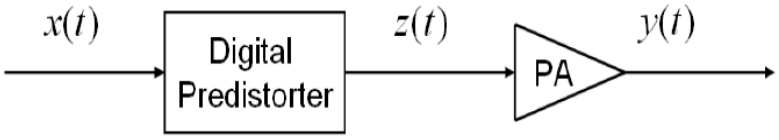

Fig.1.1 Digital Predistortion

For the realization of DPD we use the indirect learning approach (ILA) which requires only the input and output of PA for estimating the coefficients [7]. In ILA first we estimate a post-distorter and this post-distorter is then used as a predistorter. The memory polynomial model is usually used for the modelling of DPD. The nonlinearity order and memory depth of the memory polynomial PD depends upon the PA nonlinearity to be compensated and varies with the PA. There is always a limitation on the maximum performance that can be achieved by this conventional ILA-DPD approach. Once the ILA-DPD system converges to the best possible solution, there is no substantial improvement in the performance with any subsequent increase in nonlinearity order or memory depth.

In this paper we propose a multi stage ILA for digital predistortion which is having less computational complexity for the parameter estimation, as compared with the conventional ILA approach. The nonlinearity of PA is compensated using two or more than two stages in multistage ILA. Each stage can be modelled using a lower order memory polynomial and thus having low computational complexity. The identification complexity for conventional as well as multi-stage ILA is measured by computing the number of multipliers needed.

The remainder of this paper is organized as follows. Section II gives an overview of Wiener-Hammerstein model and section III gives the brief description related to conventional indirect learning architecture (ILA). Section IV presents the proposed identification algorithm for multi-stage PD. In Section V simulation results for proposed algorithm is presented and discussed. Finally Section VI concludes the paper.

II. WIENER-HAMMERSTEIN MODEL

The Wiener-Hammerstein model [8] is a three-box behavioural model. The Wiener-Hammerstein Model is modelled as a LTI system followed by a memoryless nonlinearity, which in turn is followed by another LTI system (see Fig.1.2). This type of configuration is generally used in satellite communication channels, where the power amplifier at the satellite transponder is driven near saturation to exploit the maximum power efficiency for the downlink [9].

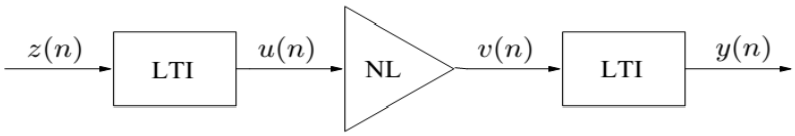

Fig.1.2 Wiener-Hammerstein Model

The subsystem model can be described as

$$u(n) = \sum_{l=0}^{L_a-1} a_l z(n-l)$$

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$$v(n) = \sum_{\substack{k=1 \\ k,odd}}^{K} b_k u(n)\,|u(n)|^{k-1}$$

$$y(n) = \sum_{l=0}^{L_c-1} c_l v(n-l) \quad (1)$$

where, $\boldsymbol{a} = [a_0, .., a_{L_a-1}]$and $\boldsymbol{c} = [c_0, .., c_{L_c-1}]$ are the impulse response values of LTI systems before and after memoryless nonlinearity respectively and $\boldsymbol{b} = [b_1, b_3, .., b_K]$ are the coefficients of the memoryless nonlinear block.

III. CONVENTIONAL INDIRECT LEARNING ARCHITECTURE (ILA)

The single stage PD identification using ILA is given in Fig.2.1. A post inverse of the PA is estimated and used as PD. The feedback path labelled "Predistorter Training" (block A) has $\frac{y(n)}{G}$ is its input in case of memoryless PA and $\frac{y(n-q)}{G}$ in PA with memory, where G is the intended power amplifier gain, and $\hat{z}(n)$ as its output. The actual predistorter is an exact copy of the feedback path (copy of A); it has $x(n)$ as its input and $z(n)$ as its output. Ideally, we would like $y(n) = G\,x(n)$, which renders $z(n) = \hat{z}(n)$ and the error term $e(n) = z(n) - \hat{z}(n) = 0$. Given $y(n)$ and $z(n)$, this structure enables us to find the parameters of block A directly, which yields the predistorter. The algorithm converges when the error energy $||e(n)||^2$ is minimized [6].

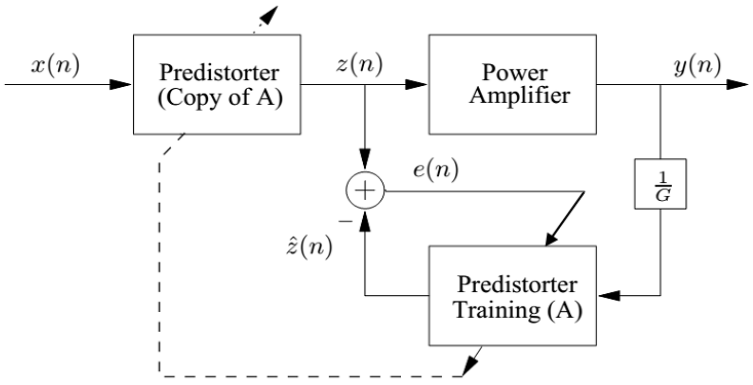

Fig.2.1 Conventional Indirect Learning Approach

A. *Memory polynomial Predistorter Design*

The memory polynomial predistorter [10] in the training branch can be described by

$$\hat{z}(n) = \sum_{k=1}^{K}\sum_{q=0}^{Q} a_{kq}\, y(n-q)|y(n-q)|^{k-1} \quad (2)$$

where $y(n)$ and $\hat{z}(n)$ are, respectively, the input and output of the predistorter in the training branch, and a_{kq} are the coefficients of the predistorter. K is the maximum order of memory polynomial and Q denotes maximum memory depth of polynomial. We take even-order nonlinear terms also for the estimation of predistorter since the addition of even-order

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terms gives a rich basis set and can provide good predistortion results without using higher order polynomials [11]. Based on a set of PA input $\{z(n_i)\}_{i=1}^{N}$ and output $\{y(n_i)\}_{i=1}^{N}$ measurements, the solution can be obtained for the predistorter coefficients, $\boldsymbol{a} = [a_{10}, a_{20}, \ldots . a_{KQ}]^T$. Once the coefficients $\{a_{kq}\}$ are found then they are plugged into the predistorter:

$$z(n) = \sum_{k=1}^{K}\sum_{q=0}^{Q} a_{kq}\, x(n-q)|x(n-q)|^{k-1} \tag{3}$$

The memory polynomial predistortion requires generation of a new sequence from power amplifier output which is given as,

$$u_{kq}(n) = \frac{y(n-q)}{G}\left|\frac{y(n-q)}{G}\right|^{k-1} \tag{4}$$

at convergence, we should have

$$\boldsymbol{z} = \boldsymbol{U}\boldsymbol{a} \tag{5}$$

where

$$\boldsymbol{z} = [z(0), z(1), \ldots . , z(N-1)]^T$$
$$\boldsymbol{U} = [\boldsymbol{u_{10}}, \boldsymbol{u_{20}}, \ldots , \boldsymbol{u_{K0}}, \ldots \boldsymbol{u_{1Q}}, \ldots \boldsymbol{u_{KQ}}]$$
$$\boldsymbol{u_{kq}} = [u_{kq}(0), \ldots \ldots , u_{kq}(N-1)]^T$$
$$\boldsymbol{a} = [a_{10}, \ldots .. a_{K0}, \ldots , a_{1Q}, . . , a_{KQ}]^T$$

The least squares solution for (5) is given by

$$\hat{\boldsymbol{a}} = (\boldsymbol{U}^H\boldsymbol{U})^{-1}\boldsymbol{U}^H\boldsymbol{z} \tag{6}$$

where $(.)^H$ denotes complex conjugate transpose. But implementing matrix inverse in real time applications is not feasible and the digital signal processor precision may impact the accuracy of the resulting matrix inverse which may reduce the performance of predistorter. For estimating the inverse we go for pseudo inverse methods like Singular Value Decomposition (SVD), QR Decomposition etc. SVD and QR give same results but the computations required to find the predistortion coefficients in SVD is high compared to QR Decomposition since SVD requires the computation of Eigen Values and Eigen vectors.

B. QR Decomposition

Mathematically any matrix A can be written as

$$\boldsymbol{A} = \boldsymbol{Q}\boldsymbol{R} \tag{7}$$

where **R** is an upper triangular matrix with $r_{ii} > 0$ and **Q** is an orthogonal matrix. An orthogonal tensor **Q** satisfies the necessary and sufficient conditions of $\boldsymbol{Q}^T\boldsymbol{Q} = \boldsymbol{I}$. For a square matrix **A**, the simultaneous equations $\boldsymbol{A}\boldsymbol{x} = \boldsymbol{b}$ can be solved by the QR decomposition, $\boldsymbol{A} = \boldsymbol{Q}\boldsymbol{R}$ as [12].

$$\begin{aligned} \boldsymbol{A}\boldsymbol{x} &= \boldsymbol{b} \\ \boldsymbol{A}^T\boldsymbol{A}\boldsymbol{x} &= \boldsymbol{A}^T\boldsymbol{b} \\ \boldsymbol{R}^T\boldsymbol{Q}^T\boldsymbol{Q}\boldsymbol{R}\boldsymbol{x} &= \boldsymbol{R}^T\boldsymbol{Q}^T\boldsymbol{b} \\ \boldsymbol{R}^T\boldsymbol{R}\boldsymbol{x} &= \boldsymbol{R}^T\boldsymbol{Q}^T\boldsymbol{b} \quad (\boldsymbol{Q}^T\boldsymbol{Q} = \boldsymbol{I}) \\ \boldsymbol{R}\boldsymbol{x} &= \boldsymbol{Q}^T\boldsymbol{b} \end{aligned} \tag{8}$$

Solving the equation 8 using back substitution gives the estimates for $\boldsymbol{x}$.

IV. MULTI-STAGE INDIRECT LEARNING ARCHITECTURE

The proposed multi stage ILA DPD is shown in Fig.4.1. The propose algorithm relies on the idea of gradually linearizing the power amplifier. The algorithm estimates the PD close to PA first and farthest from PA is estimated last. Once a predistorter stage is estimated, it is considered as a part of a new system, the cascade with PA and previous estimated stages. So for the identification of stage, P_i, we need stages P_{i-1}, P_{i-2},… P_1 and their coefficients are kept constant till we

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get convergence. The block diagram of the multistage ILA is shown in Fig 4.1. For identification of each stage more than more than one system level iteration is needed. After the convergence of a stage we can proceed with the identification of next stage.

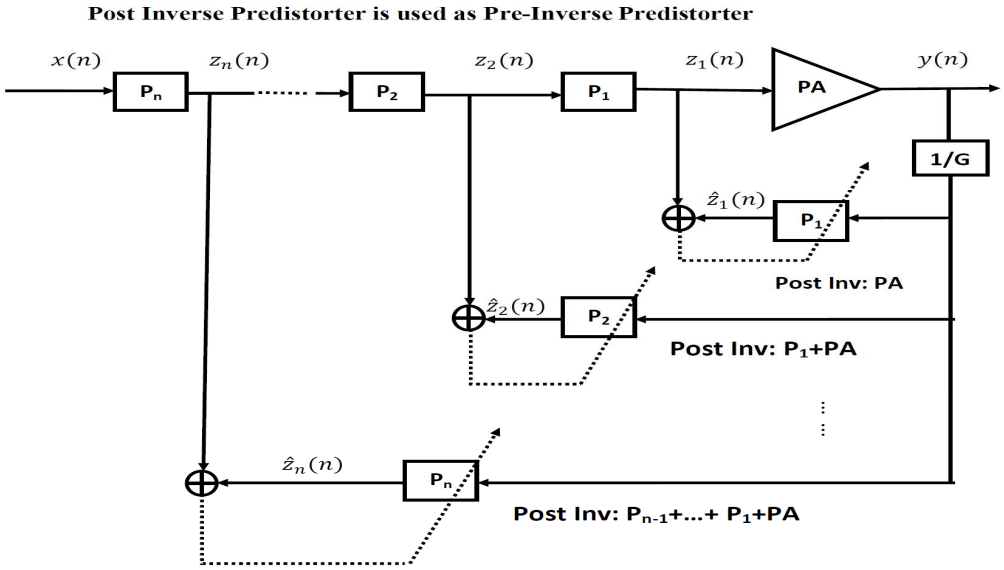

Fig 4.1. Indirect learning architecture of a multi-stage DPD

Fig. 4.2 describes this algorithm for a 3 stage DPD, where the dark boxes represent the stages that are currently being identified. For the first iteration stage 1 is identified. In second iteration, the stage 1 cascade with PA is considered for linearization and estimates the second stage. This process continues and in third iteration stage 3 of DPD is identified.

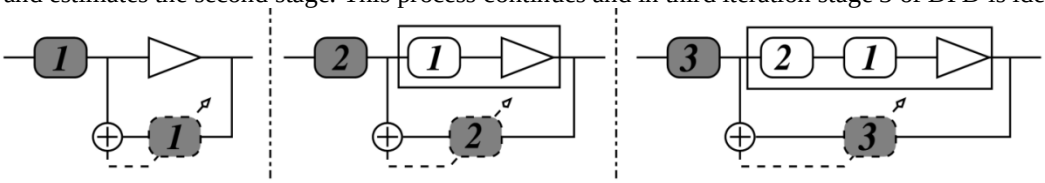

Fig 4.2. Graphical illustration of Multi-stage ILA algorithm with 3 stage PD.

V. SIMULATION RESULTS

In this section we present and analyse the simulation results for multi-stage ILA. The two LTI systems in W-H model are given as $H(z) = 0.8 + 0.1z^{-1}$ and $G(z) = \frac{3.2}{1+0.2z^{-1}}$ where $H(z)$ denotes the LTI block before memoryless nonlinearity and $G(z)$ is the LTI block coming after memoryless nonlinearity. The memoryless nonlinearity is taken as Rapp Model. The Rapp Model is a memoryless power amplifier model developed for solid-state power amplifiers (SSPA). The input output relation of Rapp model is given as

$$V_{out} = \frac{V_{in}}{\left(1 + \left(\frac{|V_{in}|}{V_{sat}}\right)^{2P}\right)^{1/(2P)}} \quad (9)$$

where V_{sat} is the saturation voltage of power amplifier and P is the smoothness factor which determines the extend of nonlinearity. The PA is driven by an OFDM signal as input; having a bandwidth of 20MHz. the DFT/IDFT size is taken as

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64 with 56 subcarriers used for transmitting data. The OFDM is oversampled by a factor 4 and is then passed through a raised cosine filter having a roll off factor $\alpha = 0.5$. For simulations the smoothness factor P of Rapp model is taken as 2 and V_{sat} is taken to be 1V. Table 5.1 shows the results for a PA modelled as Wiener-Hammerstein model. K and Q are highest order of memory polynomial and maximum memory depth respectively. The CC of two-stage ILA has been normalized with respect to conventional ILA.

Table 5.1: Identification of Memory Polynomial Predistorter using different approaches

Parameters	Without DPD	Conventional ILA	Multi-stage ILA
Index array for Nonlinearity and Memory	NA	K=[1,2,3,4,5] Q=[0 ,1,2,3,4,5,6,7,8,9,10]	Stage 1: K=[1,2,3,4,5], Q=[0,1,2,3,4] Stage 2: K=[1,2,3,4,5], Q=[0,1,2]
Number of Coefficients	NA	55	Stage 1: 20 Stage 2: 15
Normalized Complexity	NA	1	Stage 1: 0.3636 Stage 2: 0.2727

Figure 5.1 and 5.2 shows the spectral regrowth suppression capabilities of single stage memory polynomial PD and multi stage polynomial PD respectively. As observed from the plot, the memory polynomial predistortion can attain achieve sufficient amount of spectral regrowth suppression with single stage or with multi stage. Also it can be inferred from plots that for a PA with memory a memory less predistorter can attain only limited performance as compared with the performance of a memory polynomial predistorter.

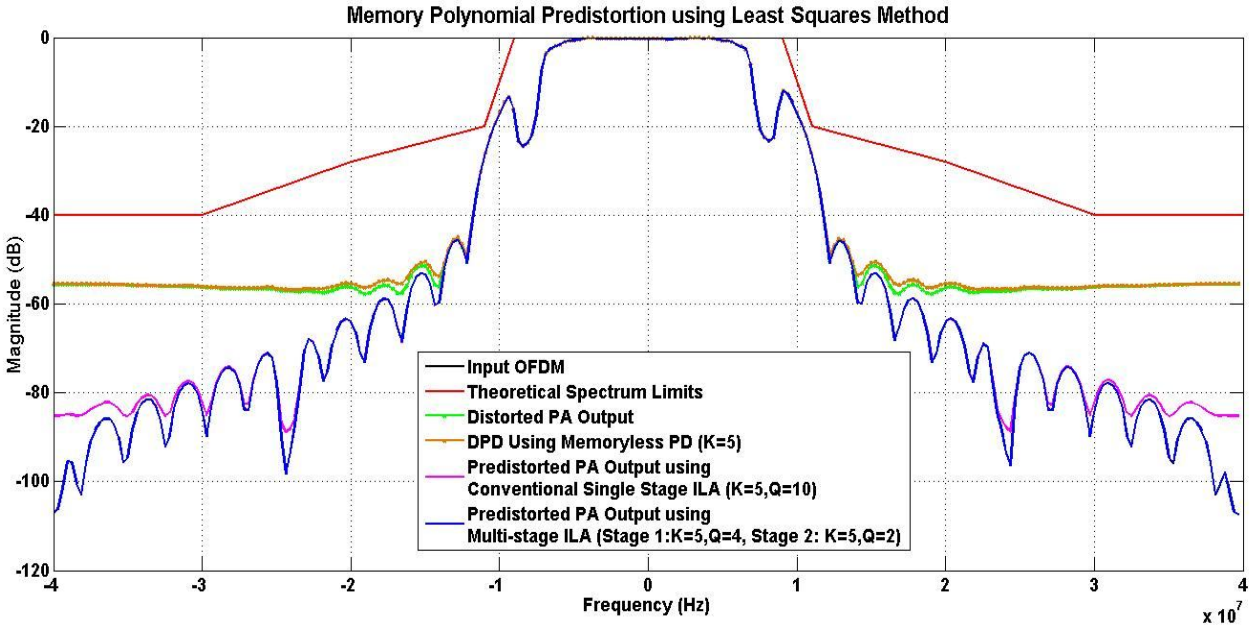

Figure: 5.1 Spectrum plot of memory polynomial predistortion using Least Squares.

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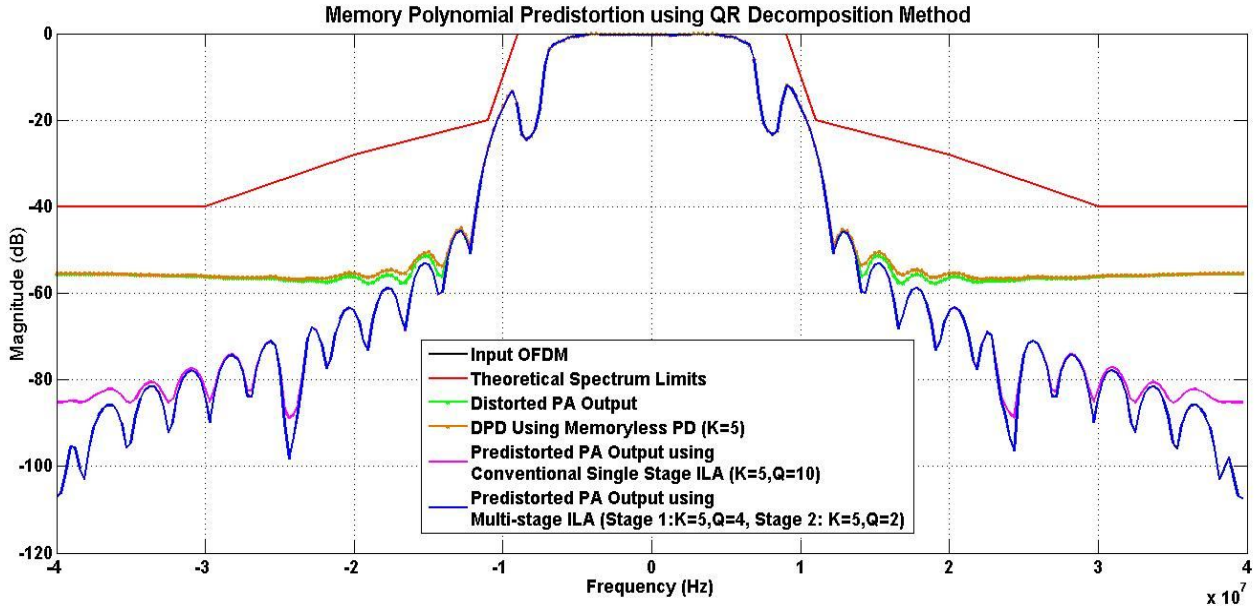

Figure 5.2 Spectrum plot of memory polynomial predistortion using Least Squares.

From the spectrum plots it can be inferred that the spectral regrowth capabilities of the two stage ILA approach is higher than that of conventional single stage approach. The two stage approach can almost suppress all the spectral broadening with less complexity.

VI. CONCLUSION

In this paper we proposed a multi-stage indirect learning architecture (ILA) with low identification complexity. The multi-stage ILA, PD is implemented in two or more stages. The reference PA model used for simulation is Wiener-Hammerstein model. The spectral regrowth suppression capability is considered for analysing the performance of the two approaches. It was shown that this multi-stage ILA was able to achieve same or even better performance than the conventional ILA but with significantly lower identification complexity.

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