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# SINGLE BIT ERROR DETECTION IN VLSI CIRCUIT

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**Abstract -** This paper examines the effect of new technology trends such as less power consumption and smaller chip feature size on very large scale integration devices. The conventional way of detecting soft error is to save one parity bit with each message word and by checking the parity bit at the output we can detect the soft error. But in proposed method, an approach is provided which can be applied on previously saved data and afterwards error can be detected. In this method 64 bit data is saved in a VLSI chip and then 8 bit parity sequence of this data is generated. After sometimes due to some transient changes like alpha particles from package decay, cosmic rays emission and thermal neutrons, error may be generated in that saved data of 64 bit. The proposed method can be used to detect a single bit soft error from the saved data by using the parity detection method.

**Keywords**— Neutron, cosmic rays, parity bit and soft error

## I. INTRODUCTION

In recent times due to technological advancements, the performance of integrated circuits has increased a lot also lower device sizes, low power consumption have also helped to improve the performance of the devices. But on the other hand, modern devices have become more susceptible to transient faults and when these faults are executed, it creates soft errors. So soft errors are errors which are not consistent rather they are random. Although Soft errors cannot damage the physical hardware of the chip however they can corrupt the value stored in the chip. Hard errors are related to the system hardware. So the difference between soft errors and hard errors is that, soft errors can be corrected by applying different techniques where as to rectify hard errors physical changes has to be done on hardware. Soft errors can occur due to environmental conditions such as radiation flux, alpha particles, cosmic rays, power supply fluctuations, temperature, pressure, humidity and electromagnetic interference. Causes of soft errors are alpha particles from package decay and cosmic rays emissions and thermal neutrons. Alpha particles are released from radioactive atoms, they contain positive charge and kinetic energy and when it travels through the semiconductor it can disturb the electron hole pair distribution. By this the digital signal can change from 0 to 1 or vice versa.

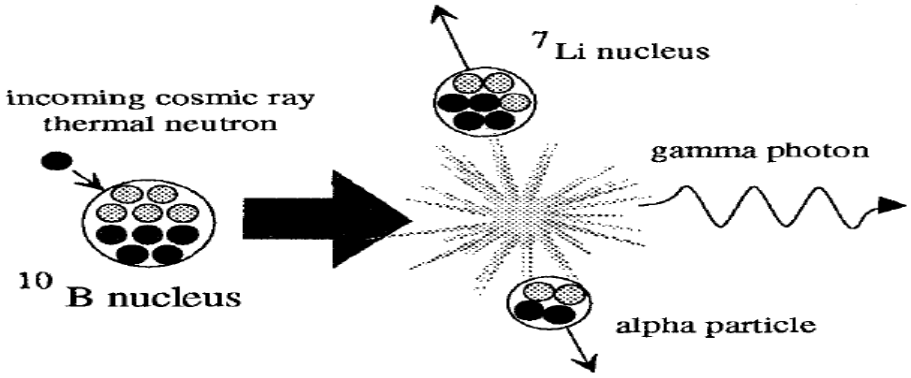


Figure 1 - Creation of soft errors due to cosmic rays, alpha particles etc.

Cosmic rays can also cause soft errors. Large part of the earth's surface contains energetic neutrons. The flux of these energetic neutrons is called cosmic rays. Cosmic rays flux depends on altitude. So at higher altitudes a system can suffer more soft errors compared to sea level.

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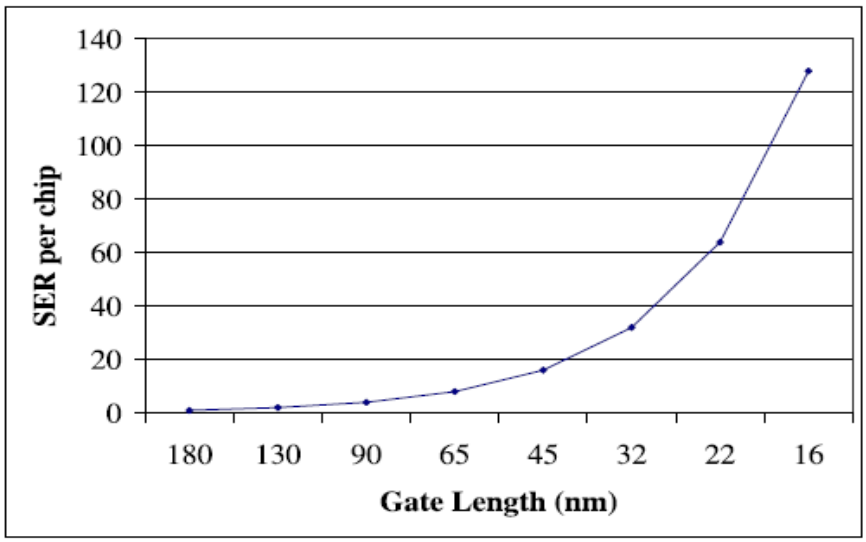


Figure 2 - Impact of SER due to gate length scaling in nm

Figure shows the soft error rate of VLSI circuits which has been growing exponentially due to technology advances. Figure shows that as the Gate length is decreasing the soft error rate is increasing. Soft errors occur when an energetic neutron coming from alpha particles strikes a silicon chip and disturb the electron hole distribution of the chip. When such a high energy particle hit the diffusion region of VLSI circuits, a voltage spike may generate on the affected circuit node.

Detection of soft errors is very important in medical electronic devices and space communications. Neutrons are produced during cancer radiation therapy. These neutrons are scattered all over the equipment and walls in the treatment room. This will produce higher order of neutron flux as compared to neutron flux of normal environment. So this high order of neutron flux will cause high rate of soft errors.

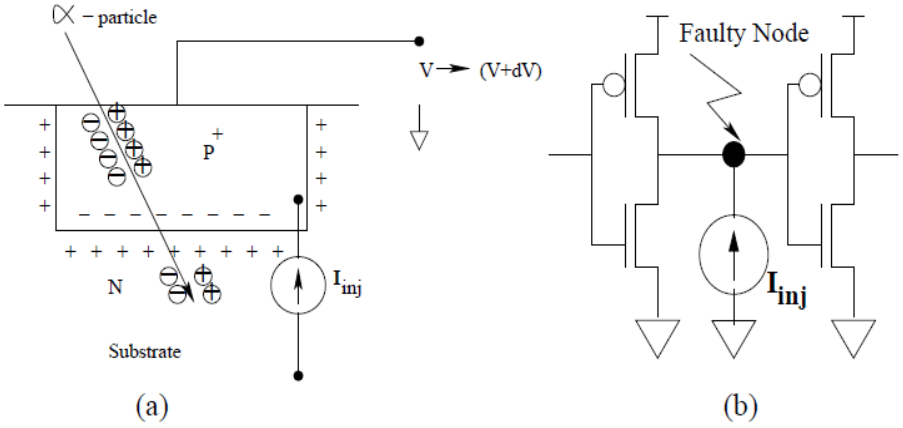


Figure 3 - (a) Alpha particle strikes on a PMOS transistor (b) Model as a current source.

When an alpha particle strikes, they generate electron hole pairs and if electric field exists then electron hole pairs will be at diffusion junction. This will create a current pulse of short duration which is called injection current. Each active node has charge and the collection of this charge is known as the collected charge. If the collected charge is equal to the critical charge, a soft error will occur. As capacitance and voltages increases Qcrit also increases and soft errors get reduced.

A. *Critical Charge* - Critical charge parameter, Qcrit is determined as the minimum electron charge that is required to alter any logic. When Qcrit parameter of a logic circuit is high, it means there is less number of soft errors because the value of capacitance and voltage is high for that logic circuit and this type of logic circuit is less susceptible to soft errors. But in other aspect when Qcrit increases, power dissipation also increases. In new technology size of chip is very small and very less supply voltages are required. In this case Qcrit will decrease. So it is very critical parameter for new technology.

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B. *Soft Error Rate* - Soft error rate is determined in terms of Mean Time between Failure (MTBF) or Failures in Time (FIT). Soft error rate is described as the rate at which a soft error can occur in a system. MTBF is determined in Years of operation.

## II. RELATED WORK

Few of the soft error mitigation techniques are discussed below:

A. *Radiation Hardening* - This involves increasing the area of basic logic gate transistors so that amount of charge accumulated is increased and current pulse generated due to ion movement is not capable of changing the state of flip flop. But major drawback of this technique is that by increasing the number of gates, the area per gate decreases hence gate density decreases.

B. *Triple Modular* - In this technique same copy of data is stored at different locations. When data retrieval takes place then it is picked up from three different locations. As probability of occurring error for same bit at all the three locations is very less, any change can be detected and corrected. But again we have to arrange for the memory space required which is three times the normal space required.

C. *SER in VLSI Circuits* - In this technique only critical variables are used instead of using whole program. This method detects soft errors at critical blocks as well as critical variables, while doing recovery erroneous variable or code block is compared with the original critical blocks as well as critical variables and if error is found it gets replaced by the original set. In this technique the program is recomputed twice if result is same it means code block is error free otherwise it detects error. Although this method requires lesser time and memory overhead by working with critical blocks and variables but this method provides less efficiency due to wrong detection of critical block. Some hardware approaches are also used but they are expensive.

## III. PROPOSED ALGORITHM

As we know the topic of soft errors now a day's attracting attention of engineers and scientists because with increase in number of gates per unit area in Integrated Circuits, the soft error rate is also increasing. The steps for removal of soft errors are generally not taken into account because under normal conditions at sea level the soft error rate is very low. But for higher altitudes, in medical premises, in air craft's & for space missions where integrated circuits are exposed to high radiation of thermal neutron flux (which in turn causes soft errors) soft error rate increases by several orders of magnitude. Thus for such operations, it is mandatory to design algorithms & implement them for removal of soft errors. Here we are suggesting a simplistic algorithmic approach implemented in C language to detect soft error by using Parity Detection Method.

Steps followed in algorithm:

1) Set count=0, y=0
2) Repeat step 3 to 6 for row=0 till row<=7
3) Repeat step 4 and 5 for column=0 till column<=7
4) if(block[row][column]==1)
then count=count+1
[End of if]
5) if(count%2==0)
Set parity1[row]=0;
else
Set parity1[row]=1;
[End of if]
[End of step 3 inner loop]
6) Set count=0;
[end of step 2 outer loop]
7) Take input of the row and column for introducing single bit error
8) Take input of a binary value
9) Repeat step 3 to 6 for row=0 till row<=7
10) Repeat step 4 and 5 for column=0 till column<=7
11) if(block[row][column]==1)
then count=count+1
[End of if]

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12) if(count%2==0)
Set parity2[row]=0;
else
Set parity2[row]=1;
[End of if]
[End of step 10 inner loop]
13) Set count=0;
[end of step 9 outer loop]
14) Repeat step 15 for i=0 till i<=7
15) if(parity3[i]==1)
then error is in bit i
[End of if]
[End of step 14 loop]
16) Repeat step 17 and 18 for i=0 till i<=7
17) if(parity3[i]==0)
then Set y=y+1
[End of if]
[End of step 14 loop]
18) Repeat step 19 and 20 for i=0 till i<=7
19) if(parity3[i]==0)
then Set y=y+1
[End of if]
20) if(y==8)
then No Error
[End of if]
[End of step 16 loop]
21) Exit

A. *Algorithm Explanation* - Suppose block is a two dimensional array and we have to find the block in which an error has occurred. To begin with, we will find the parity of the array (refer as parity '1') through steps 2 to 6 and then we will take input of the row and column from the user for introducing a single bit error in the array. After that, we will input a binary value to replace the previous binary value at the user specified location through steps 6 to 7. After introducing the single bit error, we will find the new parity of the array (refer as parity '2') through steps 9 to 13. Now we will compare parity '1' and parity '2' and find parity '3' in step 14 to 15. Finally, through step 16 to 20 we will find out the block in which the error has occurred.

B. *Discussion* - My proposed work is in the use of parity detection method in detecting soft errors in VLSI chip. In this method, we are proposing a technique which can be applied on previously saved data and errors can be detected. Firstly, for the saved data the parity sequence (parity '1') is generated and saved, this parity sequence will be $1/8^{th}$ in size for 8 bit word size. $1/16^{th}$ in size for 16 bit word size and so on. This parity data remains saved in memory. (We can also save this parity data on more than one location as it takes very less space). As we have already discussed in this paper, soft error may get introduced in the saved data due to various causes, so after some time we need to check for the soft error by again generating parity data (parity '2'). Now we will perform EX-OR operation between previously saved parity data (parity '1') & the newly generated parity data (parity '2'). If there is no soft error then result of EX-OR operation will be zero. Otherwise if there are non-zero positions in the result then these positions will be giving us the address of memory location where soft error has been occurred.
Let's take an example: Suppose we have 64 bit saved data in chip which is of 8 bit blocks. Then calculate parity sequence of each 8 bit block. Now the parity sequence of 8 bit is generated as given below.

| Original Data- 64 Bits | Parity Bits |
|---|---|
| 01111010 | 1 |
| 01010101 | 0 |
| 11010100 | 0 |
| 01010101 | 0 |
| 10101010 | 0 |
| 01010101 | 0 |
| 10101010 | 0 |
| 01010101 | 0 |

Now assume one soft error has occurred in this saved 64 bit data due to radiations or cosmic rays emissions etc. Again an 8 bit parity sequence is generated for that corrupted data as given below.

| Corrupted Data- 64 Bits | Parity Bits |
|---|---|
| 01111010 | 1 |
| 01010101 | 0 |
| 11010100 | 0 |
| 0101010**0** | **1** |
| 10101010 | 0 |
| 01010101 | 0 |
| 10101010 | 0 |
| 01010101 | 0 |

Then comparing original 8 bit parity sequence and corrupted 8 bit parity sequence by using X- OR operation, we will detect the block that is erroneous.

Original Parity Bits- 10000000 (8 Bits)
Corrupted Parity Bits- 10010000 (8 Bits)
After X-OR Operation 000**1**0000 (8 Bits)
Result- Error is in **3rd** Block.

## IV. ADVANTAGES

- Very Efficient as it uses only single bit & requires less number of X- OR gates to generate bits
- Less Time Consuming
- 'Whole' data is considered instead of a 'Critical Block'
- Cost Effective
- Simplistic Approach

## V. CONCLUSIONS

As technology advances, the problem of soft errors is spreading widely. So some techniques are required which can reduce the existing soft errors and increase the performance as well as reliability of a system. Proposed method can detect the soft error very efficiently and it is very less time consuming as well as cost effective. It uses only single bit to detect error and requires less number of EX-OR gates to generate bits.

In proposed method we have developed an algorithm in C language. This method uses 64 bits saved data and generates 8 bit parity sequence. After some time again 8 bit parity sequence is generated from 64 bit saved data. Then to examine whether an error occurred or not, EX-OR operation is performed between both parity sequences. As revealed in the example, on performing EX-OR operation between original parity sequence and corrupted parity sequence it is clear that 4th bit is non-zero. So it suggests that soft error is in 3rd block. This proposed method helps us in only detecting the soft errors however in future more work can be done so as to correct the identified soft error by using various error correcting codes such as hamming code etc.

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## BIOGRAPHY

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