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Non-Carrier based Digital Switching Angle Method for 81-level Trinary Cascaded Hybrid Multi-level Inverter using VHDL Coding

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ABSTRACT: In this paper, non-carrier based digital switching functions and patterns are developed using VHDL language (DSFPV).Non-Carrier based switching angle method is selected for the reduced distortion characteristics. Different methods of switching angle methods like equal phase method, half equal phase method, half height method and feed forward method are designed and developed using VHDL coding. These generated digital switching pulses are validated by interfacing with the 81-level Trinary Cascaded Hybrid Multi-Level Inverter (TCHMLI) simulink model. The obtained simulation results are analysed by the measure of Total Harmonic Distortion (THD), Peak Voltage (Vpeak), Root Mean Square Voltage (Vrms), Average Voltage (Vavg), Form Factor(FF) and Crest Factor(CF).

KEYWORDS: Trinary cascaded hybrid multi-level inverter, switching angle methods, VHDL code, THD

I.INTRODUCTION

Multi-level inverter is a device that converts Direct Current (DC) to Alternating Current (AC) with number of levels resembling the sine wave. A multi-level power converter is an alternative in high power and medium voltage applications. Multi-level inverter has several advantages in the field of power electronics like reduction in switching losses, lower THD, enhanced Electro Magnetic Compatibility (EMC), reduced Electro Magnetic Interference (EMI) and higher efficiency. The reduction of THD depends on the topology of multi-level inverter, its modulation schemes and switching methods.

Multilevel voltage source inverter has arrangement of semiconductor switches and DC sources. The switches are controlled to generate pulsed output sinusoidal waveform. Mostly switches in MLI are controlled by PWM strategies. PWM switching control strategy enables the MLI to reach high voltage with low harmonics without the use of the transformers. Increase in the number of voltage levels decreases the harmonic distortion of the output. Reduction in harmonics distortion decreases losses and heat in motor drive applications.

II.RELATED WORK

Different MLI topologies are designed which optimizes the power usage of the overall system by utilizing distinct type of semiconductor and modulation strategies. A fundamental issue for a multilevel inverter is to find the switching angles (times) of the inverter power switches that produce the required fundamental voltage and at the same time eliminate or reduce the values of undesired specific low order dominant harmonics. Reduction of THD can be achieved by using Mixed Integer Linear Programming (MILP) method at cost of high switching losses [1], switching angles formulated by Fourier Series method [2] and the selective harmonics elimination method [3]. The MILP method aims to minimize low order non-triplen odd harmonics starting from the 5^{th} harmonic. The triplen odd harmonics are self cancelled in the output line voltage assuming a star connected three phase inverter. The total harmonic distortion percentage (%THD) as well as the weighted total harmonic distortion percentage (%WTHD) is calculated from the 5^{th} harmonics [1]. Switching angles formulated by Fourier series method can increase the number of voltage levels and lower harmonic distortion with the same topology. The increase in the number of voltage levels leads to an improvement in power quality and reduction on the size and power loss of filter [2].The VHDL codes are used in

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generation of modulating sinusoidal wave and carrier triangular wave for pulse width modulation to generate switch patterns [4].The switch patterns were logically generated using c-code based on resultant theory [5] had advantage of higher order harmonic reduction compared to the numerical method using newton raphson method. In this paper, a digital mode of controlling the switches is designed to improve the performance of the whole system in terms of THD and high power ratings.

III.TRINARY CASCADED HYBRID MULTI-LEVEL INVERTER

Muli-level inverters are classified as (i) Diode Clamped type (ii) Flying Capacitor type (iii) Cascade type and (iv) Hybrid type. Trinary Cascaded Hybrid Multi-Level Inverter (TCHMLI) is a hybrid type which uses unequal DC link sources in each of its H-bridge circuits. Cascaded type trinary hybrid multilevel is used in this work as they require less number of components than the other types. Cascaded MLI consists of a series of H-bridge inverter units which synthesize a desired voltage from each separate DC source load voltage. TCHMLI never uses clamping diode and flying capacitor in its circuit. TCHMLI uses less number of redundant components, a modular structure, no issue of voltage balancing, and level extend is very simple [6].

In this work, a single phase TCHMLI is used to generate the 81-Levels DC link voltages in the ratio of 1:3:9:.....:3^{i-1}; where "i" is the number of H-bridges is based on the equation.

$$\mathbf{V_{dci} = 3^{i-1}E}$$

where "V_{dci}" is the DC link voltage of the "i^{th} H-bridges".
"E" is the unit voltage.

It has four H-bridges in its structure, which has four switches and a DC link source in each H-bridge is shown below in fig.1

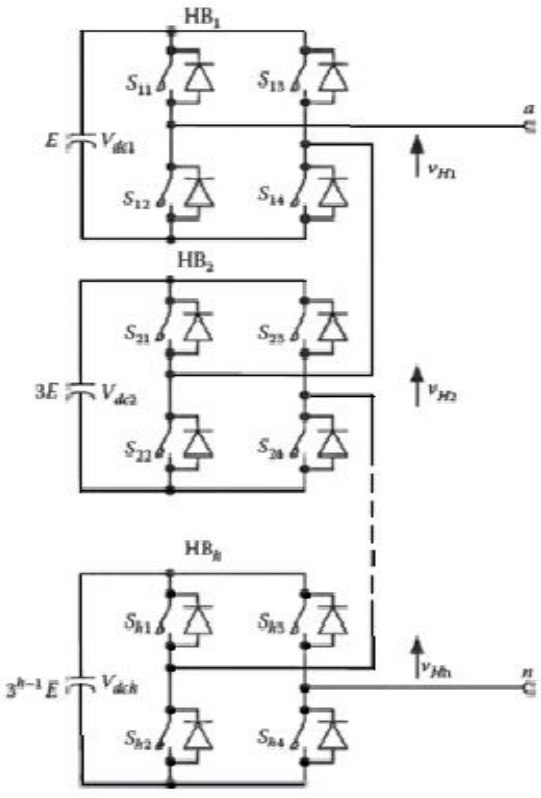

Fig.1 Trinary Cascaded Hybrid Multi-Level Inverter

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The switching functions for the 81-level TCHMLI are obtained based on the switching combinations of the DC link sources. The switching function for each H-bridge is designed to out a positive DC value when the switches S_{i1} & S_{i4} are turned ON, a negative DC value when the switches S_{i2} & S_{i3} are turned ON and a zero value when either S_{i1} & S_{i3} are turned ON or S_{i2} & S_{i4} are turned ON. Generally these switching functions are generated using pulse width modulation strategy like phase disposition, alternate phase disposition, and in phase disposition which provides high power with low harmonics [7].In this work switching functions are designed using switching angle methods. The development of switching patterns to generate 81 DC levels using switching angle method is explained in the following section.

IV. PROPOSED SWITCHING ANGLE METHOD

Multi-level inverter is designed for different topologies using several techniques with many advantages. An improper arrangement of switching angles in MLI could not generate an efficient AC output waveform. The Switching Angle method is utilized for the evaluation of angles to generate the different DC levels in the multi-level inverter and reduce THD.

The switching angle method enables the multi-level inverter to generate an output resembling the sinusoidal wave. The switching angle method is a non-carrier based method; hence no modulation schemes for the generation of switching pattern are required. Switching angle is the point or event at which the multi-level inverter proceeds from one level to the next level. The switching angle method is a technique which formulates all events that occur within one cycle to change the output of the multi-level inverter. Once all these switching angles are derived, the sequence for switch patterns is formatted as required by the type of "m-level" multi-level inverter.

The switching angle method divides the multi-level inverter output into four quadrants in angles. (i) First Quadrant (0°-90°) (ii) Second Quadrant (90°-180°) (iii) Third Quadrant (180°-270°) and (iv) Fourth Quadrant (270°-360°).The evaluations of switching angles in each of these quadrants are relatively simple and interlinked.
For "m"- level ,the switching angles in the first quadrant (0°-90°) are calculated as say $\alpha_1, \alpha_2, \alpha_3, \alpha_4, \alpha_{5,\ldots\ldots}, \alpha_{(m-1)/2,}$ second quadrant (90°-180°) as $\pi - \alpha_{(m-1)/2}, \ldots\ldots, \pi - \alpha_5, \pi - \alpha_4, \pi - \alpha_3, \pi - \alpha_2, \pi - \alpha_1$, third quadrant (180°-270°) as $\pi + \alpha_1, \pi + \alpha_2, \pi + \alpha_3, \pi + \alpha_4, \pi + \alpha_{5,\ldots\ldots\ldots\ldots\ldots\ldots}, \pi + \alpha_{(m-1)/2}$ and fourth quadrant (270°-360°) as $2\pi - \alpha_{(m-1)/2}, \ldots\ldots, 2\pi - \alpha_5, 2\pi - \alpha_4, 2\pi - \alpha_3, 2\pi - \alpha_2, 2\pi - \alpha_1$.

This switching angle estimation is validated by implementing in four methods. They are
(i) **Equal Phase Method (EPM)**: The switching angles are estimated and arranged with equal space from 0 to π.
(ii) **Half Equal Phase Method (HEPM)**: The switching angles are calculated and placed with equal space in alternate angles.
(iii) **Half Height Method (HHM)**: The switching angles are manipulated and assigned with equal space till the half of the multi-level inverter output and with equal space in alternate angles above the half of the multi-level inverter output.
(iv) **Feed Forward Method (FFM)**: The switching angles are derived and designated with equal space till the quarter of the multi-level inverter output such that the wider gap between the positive half cycle and negative half cycle is reduced than the above three methods.

V. DSFPV ALGORITHM

Very High Speed Integrated Circuit **H**ardware **D**escription **L**anguage (VHDL) allows modelling the behaviour of the required system and verifying it by simulation before getting synthesized. VHDL is used for the design of 81-Level TCHMLI. In fig.2, the DSFPV has two blocks namely Digital Switching Function using VHDL code (DSFV block) and Digital Switching Pattern using VHDL code (DSPV block) to generate the switching functions and patterns. For the 81-level TCHMLI, there are 40 switching angles in each of the four quadrants which are calculated for all the four switching angle methods. These 160 switching angles are converted into 2^9 bit equivalent. The DSFV block designed by VHDL coding, outputs the 80 voltage levels in which 40 for positive half cycle and 40 for negative half cycle as shown in Table.1

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In the DSPV block, the 80 voltage levels and a zero voltage level are combined logically to generate the patterns required for the 16-switches in the H-bridges of 81-level TCHMLI. The 16-switching patterns are interfaced with the developed TCHMLI MATLAB SIMULINK model to get the sinusoidal output with reduced THD. Fig.3 explains the design flow for DSFPV algorithm. The designed switching pattern are verified by XILINX tool in Matlab and validated by interfacing with the cascaded hybrid multi-level inverter model developed using SIMULINK. POWER SYSTEM BLOCK SET.

Table 1: DC link source combination for 81-levels TCHMLI

Positive Voltage Levels	DC link Source Combinations	Positive Voltage Levels	DC link Source Combinations
40	+1+3+9+27	20	-1+3-9+27
39	+3+9+27	19	+1-9+27
38	-1+3+9+27	18	-9+27
37	+1+9+27	17	-1-9+27
36	+9+27	16	+1-3-9+27
35	-1+9+27	15	-3-9+27
34	+1-3+9+27	14	-1-3-9+27
33	-3+9+27	13	+1+3+9
32	-1-3+9+27	12	+3+9
31	+1+3+27	11	-1+3+9
30	+3+27	10	+1+9
29	-1+3+27	9	+9
28	+1+27	8	-1+9
27	+27	7	+1-3+9
26	-1+27	6	-3+9
25	+1-3+27	5	-1-3+9
24	-3+27	4	+1+3
23	-1-3+27	3	+3
22	+1+3-9+27	2	-1+3
21	+3-9+27	1	+1

Negative Voltage Levels	DC link Source Combinations	Negative Voltage Levels	DC link Source Combinations
-40	-1-3-9-27	-20	+1-3+9-27
-39	-3-9-27	-19	-1+9-27
-38	+1-3-9-27	-18	+9-27
-37	-1-9-27	-17	+1+9-27
-36	-9-27	-16	-1+3+9-27
-35	+1-9-27	-15	+3+9-27
-34	-1+3-9-27	-14	+1+3+9-27
-33	+3-9-27	-13	-1-3-9
-32	+1+3-9-27	-12	-3-9
-31	-1-3-27	-11	+1-3-9
-30	-3-27	-10	-1-9
-29	+1-3-27	-9	-9
-28	-1-27	-8	+1-9
-27	-27	-7	-1+3-9
-26	+1-27	-6	+3-9
-25	-1+3-27	-5	+1+3-9
-24	+3-27	-4	-1-3
-23	+1+3-27	-3	-3
-22	-1-3+9-27	-2	+1-3
-21	-3+9-27	-1	-1

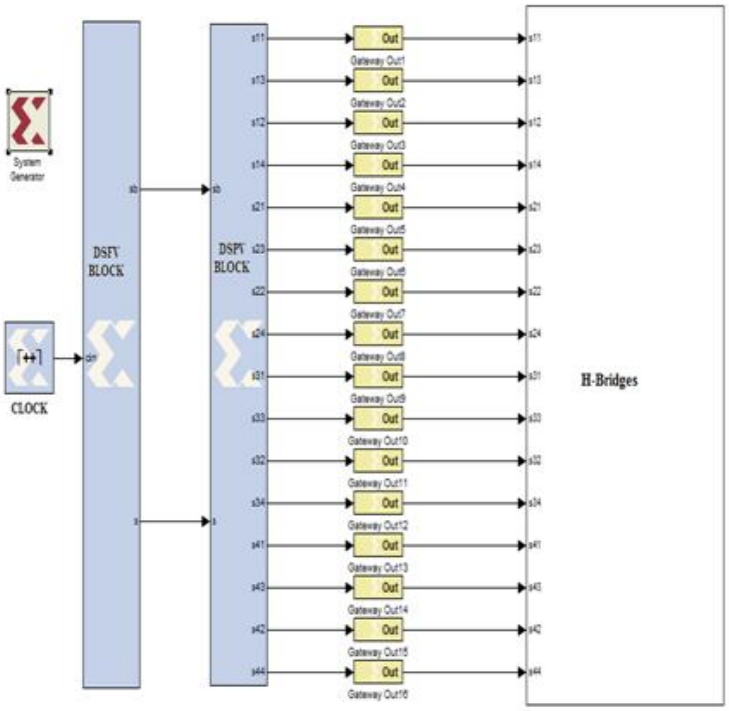

Fig.2: Matlab-Simulink model interfacing DSPFV algorithm with 81-level TCHMLI

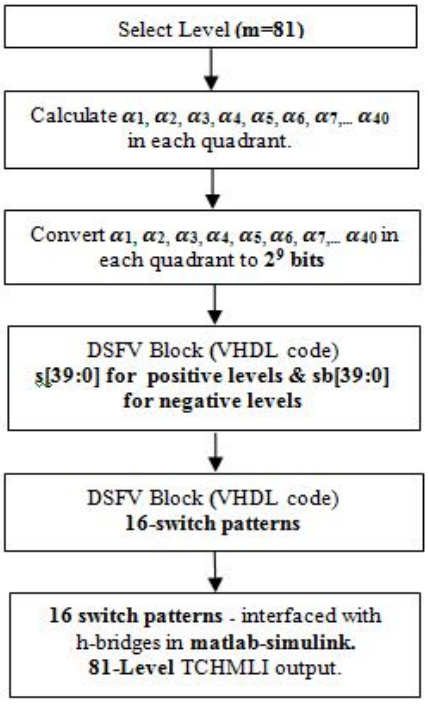

Fig .3: Design flow for DSFPV Algorithm

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VI. RESULT AND DISCUSSION

Simulation of 81-level TCHMLI is done using SIMULINK Power System Blockset. The trinary dc link sources used are V_{dc1} = 5E, V_{dc2}=15E, V_{dc3}=45E and V_{dc4}=135E V. Simulation results validating the different angle methods using the proposed DSFPV algorithm are presented.

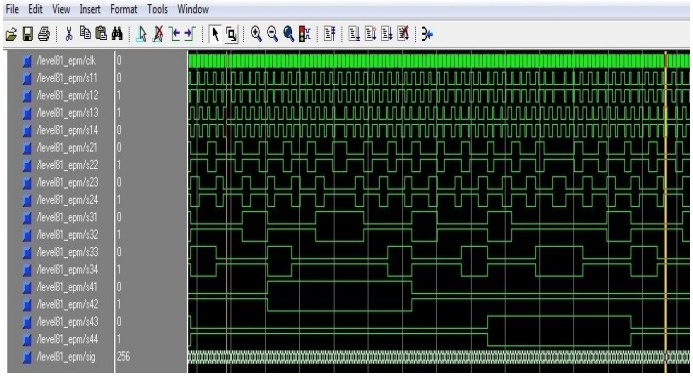

Fig. 4: Digital Switching patterns for 81-level TCHMLI using EPM

Fig.4 shows the digital switching pattern for the TCHMLI using EPM. In the EPM, the switching angles are arranged in the range of 0 to π.

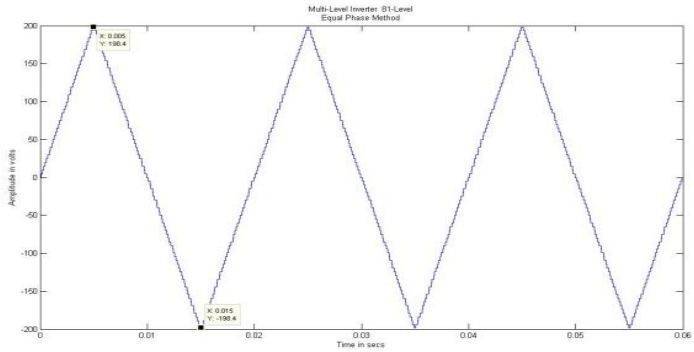

Fig. 5: Output of 81-level TCHMLI using EPM

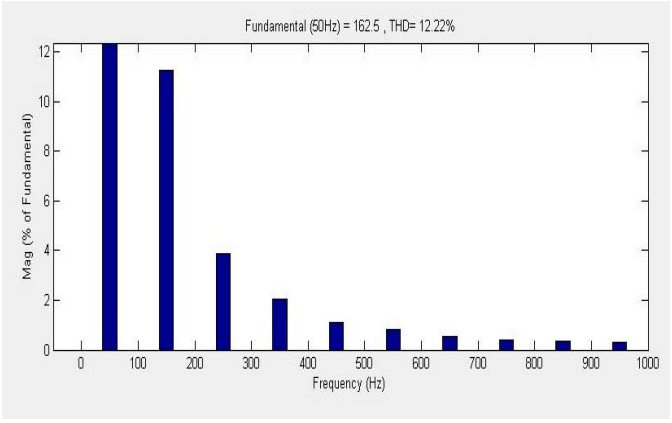

Fig. 6: THD of 81-level TCHMLI using EPM

Fig.5 and Fig.6 show the simulation output and the THD of 12.22% for the 81-level TCHMLI-EPM.

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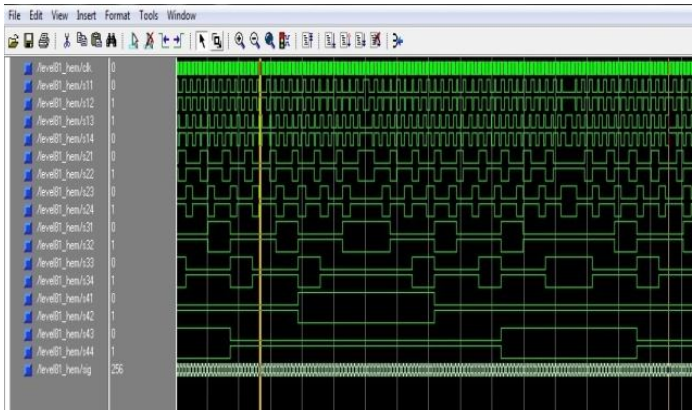

Fig. 7: Digital Switching patterns for 81-level TCHMLI using HEPM

The digital switching pattern for the 81-level TCHMLI using the switch pattern HEPM is shown in Fig.7.

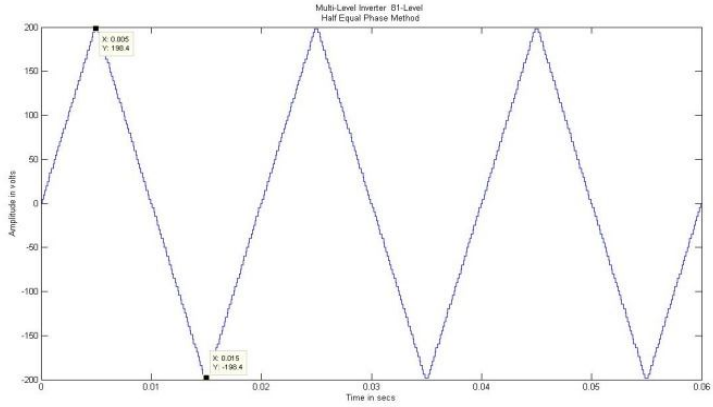

Fig. 8: Output of 81-level TCHMLI using HEPM

Fig.8 shows the 81-level output waveform of TCHMLI using the switch pattern HEPM and the THD of the HEPM is found to be 12.28% as shown in Fig.9. The simulated 81-level output waveforms of TCHMLI using EPM and HEPM depicts the fact that none of the above methods were close to a sinusoidal waveform. This problem was rectified by the design of 81-level TCHMLI using HHM.

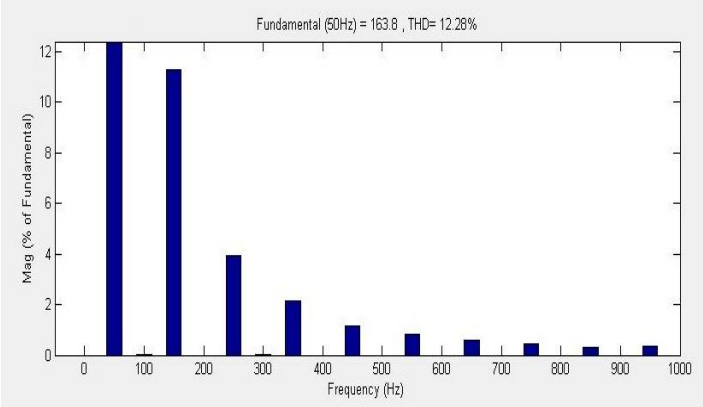

Fig. 9: THD of 81-level TCHMLI using HEPM

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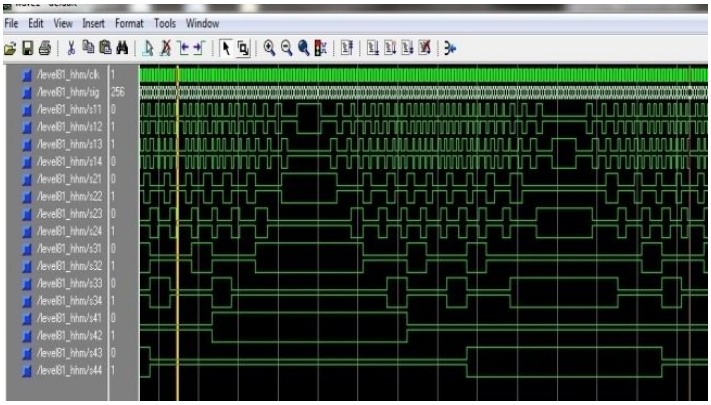

Fig. 10: Digital Switching patterns for 81-level TCHMLI using HHM

Fig.10 shows the digital switching patterns. The output obtained from the DSFPV algorithm using this method is close to a sinusoidal waveform and is shown in Fig.11 and Fig.12 shows the THD value of the HHM as 1.42%.

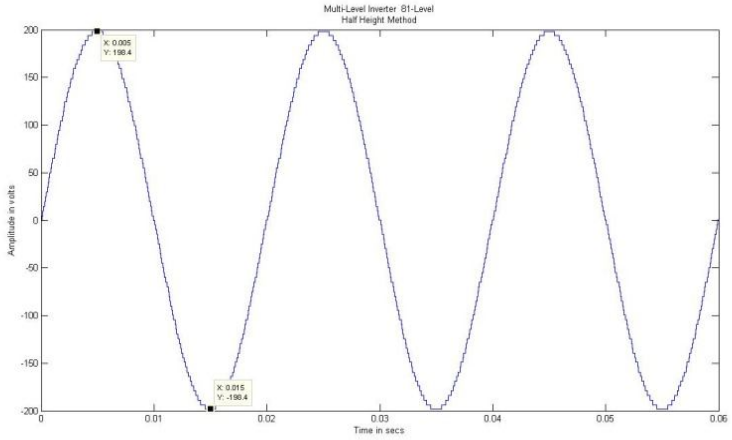

Fig. 11: Output of 81-level TCHMLI using HHM

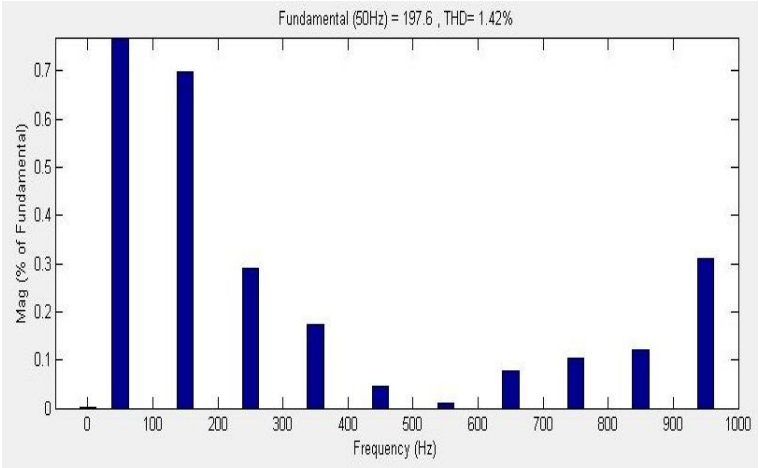

Fig. 12: THD of 81-level TCHMLI using HHM

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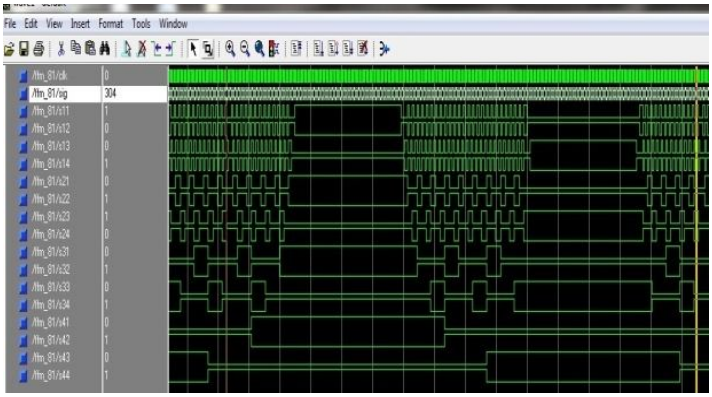

Fig. 13: Digital Switching patterns for 81-level TCHMLI using FFM

The 81-level TCHMLI is designed by using the switch pattern FFM as shown in Fig.13. The 81-level output waveform of TCHMLI using FFM is presented in Fig.14.The 81-level output waveform of TCHMLI using FFM as shown in Fig.15 has more duration for its peak level ,hence its THD is 10.33%.

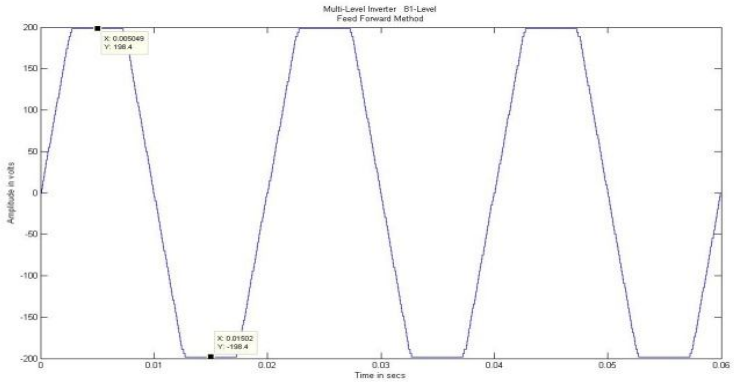

Fig. 14: Output of 81-level TCHMLI using FFM

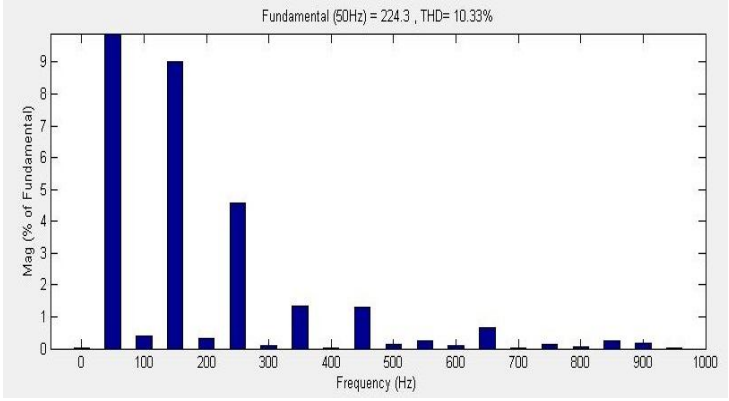

Fig. 15: THD of 81-level TCHMLI using FFM

The switching angle methods designed by DSFPV algorithm can be easily implemented using FPGA in the future. This DSFPV algorithm is flexible to synthesize and provide a new way of implementing the TCHMLI with less design complexity. The different switching angle methods are developed for the different levels say 9-level, 27-level, 81-level of TCHMLI. The simulated results for each 9,27,81-level TCHMLI are analysed by the performance measure Vpeak, Vrms, Vavg, THD,FF and CF are shown in Table 2.

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Table 2: Comparison of switching angle methods

LEVELS	LEVEL-9						LEVEL -27						LEVEL -81					
METHODS	Vpeak	Vrms	Vavg	THD (%)	FF	CF	Vpeak	Vrms	Vavg	THD (%)	FF	CF	Vpeak	Vrms	Vavg	THD (%)	FF	CF
EPM	32.53	23.02	20.71	20.96	1.11	1.414	106.5	75.31	67.8	13.53	1.11	1.414	162.5	114.90	103.45	12.22	1.11	1.414
HEPM	35.71	25.25	22.73	18.21	1.11	1.414	109	77.07	69.39	13.15	1.11	1.414	163.8	115.82	104.27	12.28	1.11	1.414
HHM	42.79	30.25	27.24	10.13	1.11	1.414	127.3	90.01	81.04	3.67	1.11	1.414	197.6	139.72	125.79	1.42	1.11	1.414
FFM	47.28	33.43	30.09	18.72	1.11	1.414	151.2	106.9	96.25	15.44	1.11	1.414	224.3	158.60	142.79	10.33	1.11	1.414

VII.CONCLUSION

In this paper non-carrier based switching angle method digital switch patterns were generated using VHDL coding to produce the sinusoidal output waveforms for improving the power quality of trinary mode cascaded hybrid type MLI. Performance factors like THD related to power quality issues and Vrms, Vavg, Vpeak related to DC bus utilization were evaluated and analysed. TCHMLI using HHM method is found to be satisfactory with more than ten times reduction of THD from 12.28% to 1.42% in 81-level MLI, from 15.44% to 3.67% in 27-level MLI, from 20.96% to 10.13% in 9-level MLI. Table 2 implies the inverse relationship between the number of levels and THD.TCHMLI using FFM method is found satisfactory for DC bus utilization. Therefore the MLI for a particular application based on output voltage quality and distortion level reduction can be selected.

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BIOGRAPHY

Joseph Anthony Prathap was born in 1981 in puducherry. He has obtained B.E [Electronics and Communication] and M.Tech [VLSI Design] degrees in 2003 and 2007 respectively from Sathyabama University. He has put in 8 years of service in teaching. He is currently research scholar in the Department of Instrumentation Engineering at Annamalai University, Chidambaram, India. His research interest includes VLSI design, development of digital switch patterns, FPGA control techniques for power converters, photovoltaic power electronics converters.

T.S.Anandhi was born in 1974 in chidambaram. She has obtained B.E [Electronics and Instrumentation] and M.E [process control and Instrumentation] degrees in 1996 and 1998 respectively and then Ph.D in power electronics in 2008 form Annamalai University. She is currently Associate professor in the Department of Instrumentation Engineering at Annamalai University, chidambaram, India and has put in 15 years of service. She has produced one Ph.D and guiding 6 Ph.D scholars. Her research interests are in power converters, control techniques for multiple connected power converters, embedded controllers for power converters, renewable energy based power converters. She is a life member of Indian society for technical education.