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MODELLING AND SIMULATION OF DIODE CLAMP MULTILEVEL INVERTER FED THREE PHASE INDUCTION MOTOR FOR CMV ANALYSIS USING FILTER

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Abstract: In this paper, we have proposed a passive filter with an objective of eliminating the common-mode and differential mode voltage generated. For determining the parameters of filter, the filter transfer function is utilized to achieve a desirable filtering performance. Simulation is carried out on a 415V/3Hp induction motor sysem to verify the validity and effectiveness of proposed filter. Multilevel inverter can synthesize switched waveforms with lower levels of harmonic distortion than an equivalently rated two-level converter. The multilevel concept is used to decrease the harmonic distortion in the output waveform without decreasing the inverter power output. The most important topologies like diode-clamped inverter (neutral- point clamped), capacitor-clamped (flying capacitor), and cascaded multilevel with separate dc sources. various modulation technique in multilevel inverter are sinusoidal pulse width modulation, selective harmonic elimination. & space vector modulation**.**

Keywords: passive filter, common-mode voltage, differential-mode voltage, Harmonics content

I. INTRODUCTION

Modern insulated gate bipolar transistors (IGBTs) rated at 600V or 1,200V have Switching frequencies of 1 to 20 kHz and rising time of 0.1µsec making it possible to use them widely in medium voltage system and a great contribution to improve the controllability of voltage , current , and torque . It also helps in reduction of acoustic noise . However, this improvement is accompanied by high dv/dt value of inverter at motor terminal subjecting the motor to stress at the switch transient and with the increase in switching frequency, the rate of application of stress on motor is increased and has been attributed to many problems, including the well-known bearing current, winding failures[1],[2] etc. Furthermore, the percentage of high common mode voltage at motor terminals has been shown to contribute to high frequency leakage current to ground as well as induce shaft voltage due to electrostatic coupling between the stator and rotor[3],[4]. While high magnitudes of leakage current to ground have been shown to interfere with ground fault protection systems in industrial facilities and contribute to wide-band electromagnetic interference (EMI) issues. The induced shaft voltages have been shown to cause bearing currents which result in pitting, fluting, and subsequent failure[5]. Filters are employed at the output of voltage source PWM inverters for the purpose of eliminating the side-effects mentioned above. Generally, the filters are classified into two categories: passive and active. So far, various types of passive filter configuration, based on inductors, capacitors and resistors or diodes, have been proposed in [6]-[11]. Ogasawarea, *et al* have proposed a circuit consisting mainly of complimentary transistors and a common-mode transformer for achieving active cancellation of common-mode voltage [11]. This method effectively eliminates the line-to-line common-mode voltage and shaft voltage, but it makes no contribution for reducing differential-mode overvoltage occurs at motor terminals when a long cable is used to connected PWM inverter and motor. At the same time, the active circuits of [11],[12] and [13] have limitations because complimentary transistors rated at 600V or higher are presently not available in the market.

In response to these concerns, this paper proposes a new inverter output terminal passive filter focusing on reducing common-mode and differential-mode voltage gradient simultaneously and detailed design procedure of parameters is given. The proposed filter consists of three inductors, three capacitors, one resistor.Compared with conventional

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passive filters, the proposed filter can suppress the dv/dt value of common-mode and differential-mode voltage symmetrically by connecting one terminal of common-mode transformer to the midpoint of dc-link.

II. COMMON MODE VOLTAGE

CMV is defined as the voltage at the star point of the load and the system ground. The magnitude of the CMV depends on grounding system.[1]

$$V_{com} = \frac{1}{3}(V_a + V_b + V_c) \quad (1)$$

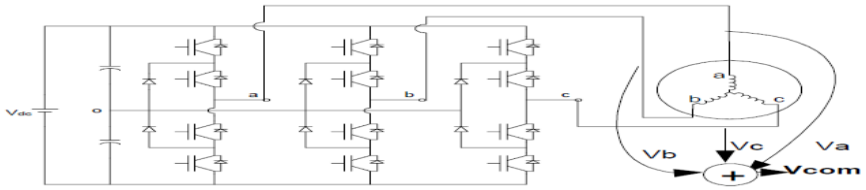

Fig. 1 Illustration of common Mode Voltage

Because of 12 switches in the Neutral Point Clamped or Diode clamped inverter shown in Fig. 1, They produce 19 output voltage vectors including a zero voltage vector. If sum of the output voltages is not zero, a common-mode voltage results. An example of waveforms of phase voltages and the resulting common-mode voltages are shown in Fig. 2

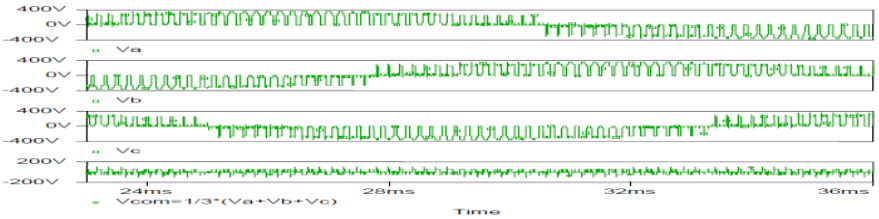

Fig. 2 Phase output voltage & common mode voltage of Neutral Point clamped or Diode clamped inverter

The Neutral Point (NP) voltage variations cause the added variations of three-phase output voltage and induce some harmonics in the output.

$$V_a' = V\ \sin(\omega t) + V_{np} \quad (2) \qquad V_a' = V\ \sin(\omega t - 120^0) + V_{np} \quad (3)$$

$$V_a' = V\ \sin(\omega t + 120^0) + V_{np} \quad (4) \qquad V_{com}' = \frac{1}{3}(V_a' + V_b' + V_c') \quad (5)$$

Finally, the NP voltage variations generate common-mode voltage at three times the fundamental output frequency, which occurs even if the high frequency and high dv/dt switching common-mode voltage is mitigated by some techniques such as filtering. When the common-mode voltage and resulting shaft voltage caused by the NP voltage variation are large enough to break the oil film insulation in the bearings, bearing currents are generated, which by erosion may cause premature failures of the motor bearings. Hence the NP voltage control is important not only for the Neutral Point Clamped or Diode Clamped inverter operation but also for common-mode voltage mitigation [5]. The shaft voltage is measured between the motor shaft and the motor frame, which is usually grounded. It is generated by the common-mode voltage coupling through the path that consists of the motor stator windings, rotor windings and the distributed capacitance between them. Its magnitude is dependent on not only the magnitudes of the common-mode voltage but also the coupling impedance[6]

III. DESIGN OF THE PASSIVE FILTER

The simple LC filter is designed to eliminate CMV and harmonic distortions. Filters are mainly classified into three categories: passive, active and hybrid. For, various types of passive filter configuration based on inductors, capacitors and resistors or diodes can be proposed. Passive filters, can suppress the dv/dt value of common-mode and

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differential-mode voltage symmetrically by connecting one terminal of common-mode to the midpoint of dc-link. The validity and effectiveness of proposed filter is supported by the simulation results carried out on 415V/3Hp induction motor. Active filters are difficult to design' so in this work focus is mainly on designing the passive filter..

In this work LC filters are used in simulation model to eliminate common mode voltage & total harmonics distortion with two level, three level and five level inverter. This LC-filter is suited to configurations where the load impedance across C is relatively high at and above the switching frequency. The cost and the reactive power consumption of the LC-filter is more than L-filter because of the addition of the shunt element

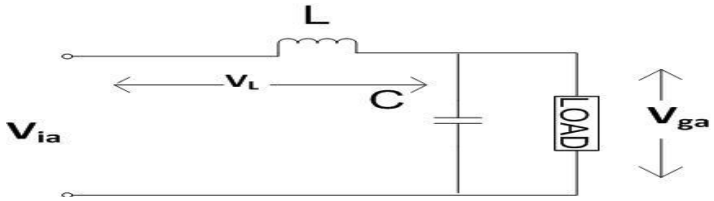

Fig. 3 L-C filter topology.

The output current ripple is the same as the inductor current ripple with an L-filter, where the attenuation depends solely on the filter inductance. The LC low pass filter is able to attenuate most low order harmonics in the output voltage waveform. To minimize distortion, for linear or non linear loads, the inverter output impedance must be minimized. Therefore the capacitance should be maximized and the inductance minimized when specifying the cut-off frequency. This decreases the overall cost, weight, volume . But by increasing the capacitance, the inverter power rating will be increased due to the reactive power increase due to the filter.

The inductor determines the ripple in the inductor current and reduces the low frequency harmonic components. Consider the inverter phase 'a' voltage Va , and assume that the output voltage Vga varies slowly relatively to the switching frequency. According to this harmonic standard, 15–20% of the rated current is allowable. The maximum ripple can now be calculated from equation given below. The ripple current depends on the DC link voltage, inductance, and the switching frequency. The DC link voltage and switching frequency are constant, thus the inductance can be calculated from equation mentioned

IV. COMMON MODE FILTER

This is one of the effective methods of reducing common mode current. The winding on the core for each phase are wound in the same direction. This cancels out the flux produced by the line currents and the flux produced due to ground currents add. Therefore the common mode choke offer ideally zero inductance to line currents and offers a high inductance to common mode currents. While constructing the CM choke one must separate the first turn from the last turn otherwise the parasitic capacitance for high frequency shunts the core which reduces its effectiveness.

V. SIMULATION AND RESULT

A) *Simulation of Two Level Diode Clamped Inverter Induction Motor without filter-*

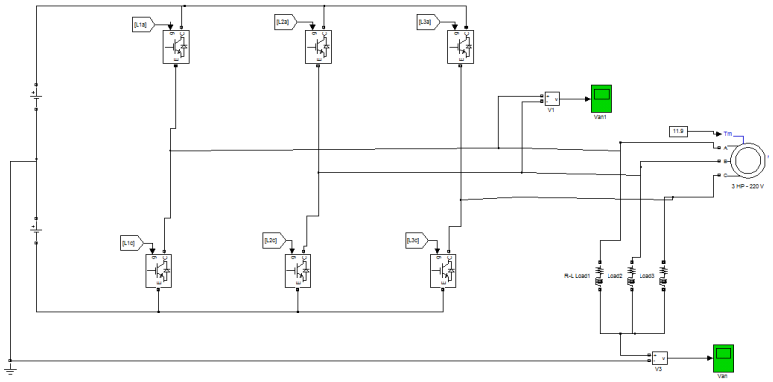

Fig. 4 Model of Two Level Diode Clamped Inverter fed Three Phase Induction Motor without filter

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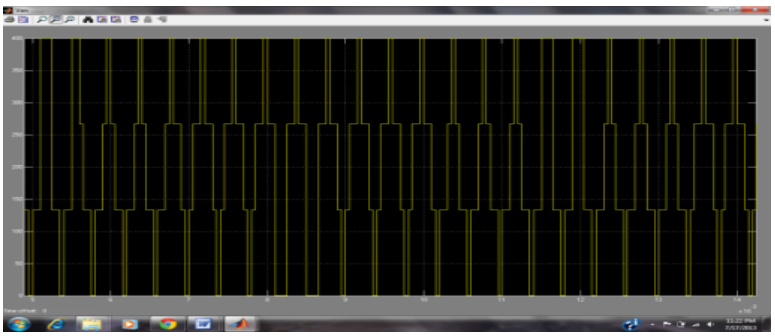

Fig. 5 CMV of Two Level Inverter without Filter.

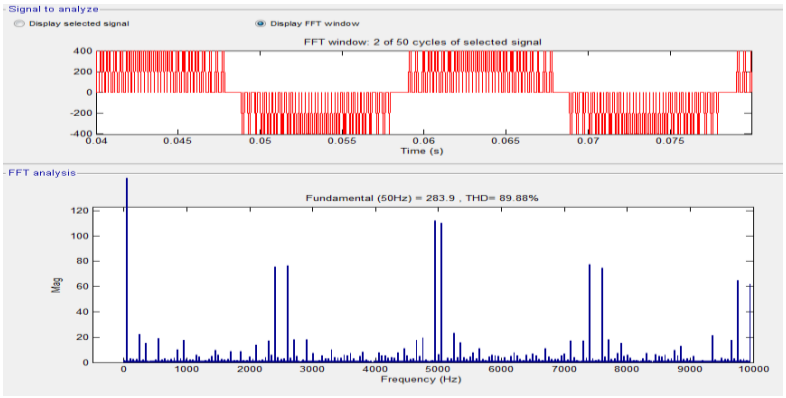

Fig. 6 Harmonic Spectrum of Two level Inverter without filter Phase Voltage at modulation Index=1

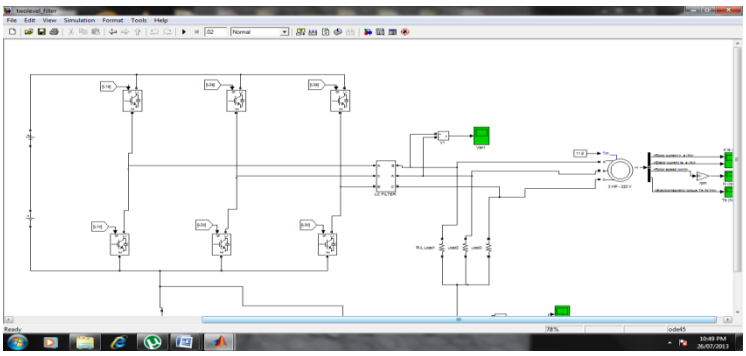

Fig. 7 Model of Two level Inverter fed induction motor with filter

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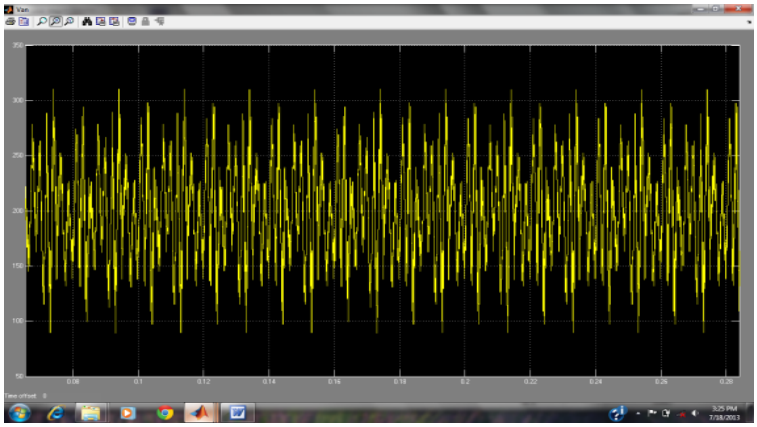

Fig. 8 CMV of Two level inveter with Filter.

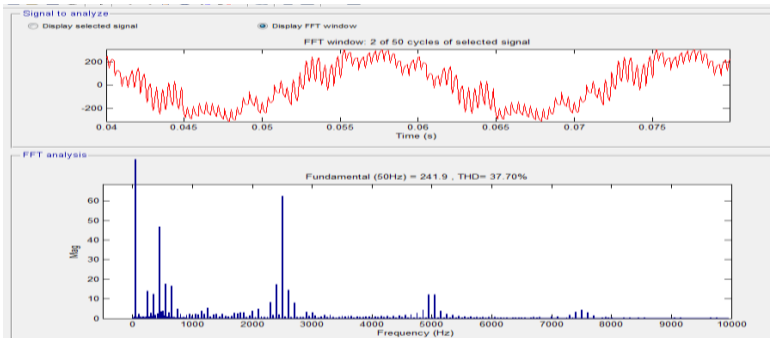

Fig. 9 Harmonic Spectrum of Two level Inverter with filter Phase Voltage at modulation Index=1

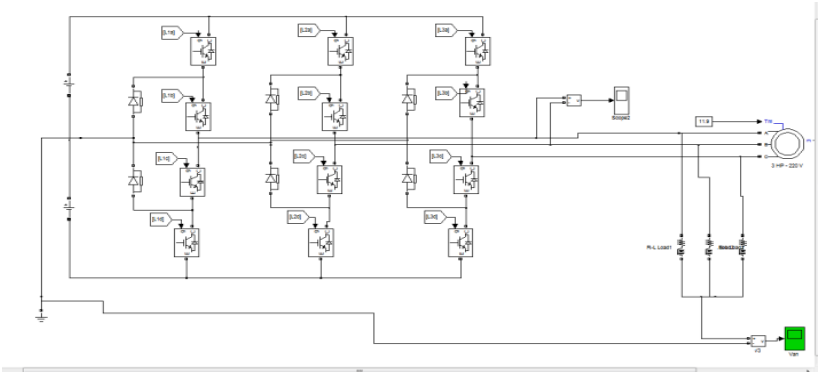

Fig. 10 Model of Three Level Diode Clamped Inverter fed Three Phase Induction Motor without filter

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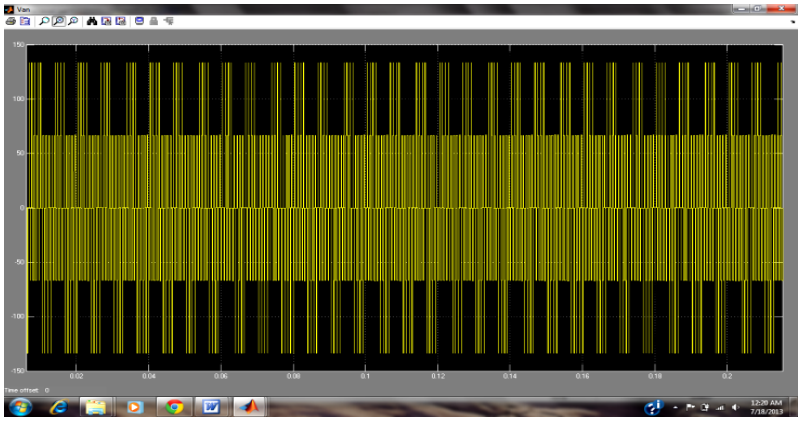

Fig. 11 CMV of Three Level Diode Clamped Inverter(PD PWM Technique) without filter

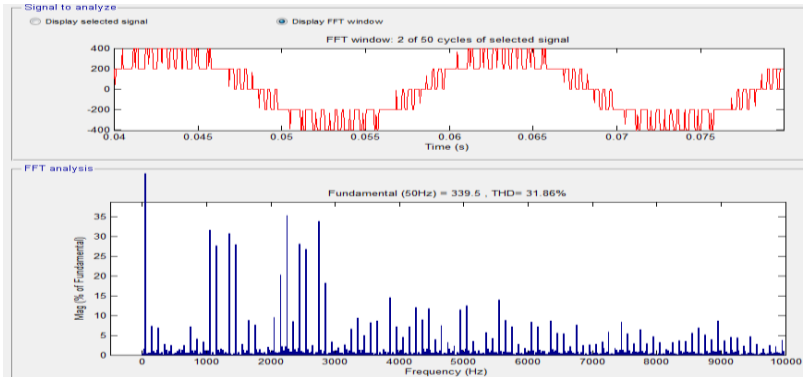

Fig. 12 Harmonic Spectrum of Three level diode clamped Inverter without filter Phase Voltage at modulation Index=1 (PD PWM Technique)

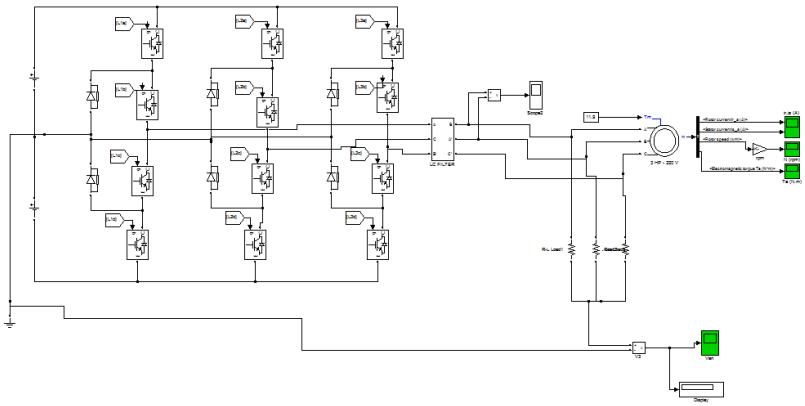

Fig. 13 Model of Three Level Diode Clamped Inverter fed Three Phase Induction Motor with filter

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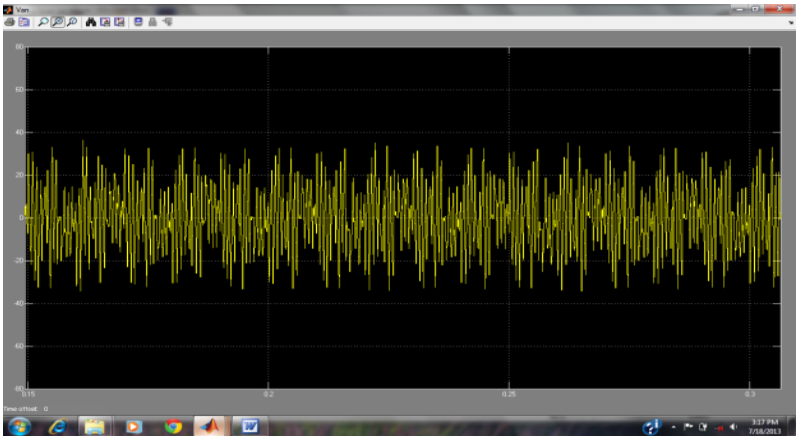

Fig. 14 CMV of Three Level Diode Clamped Inverter(PD PWM Technique) with filter

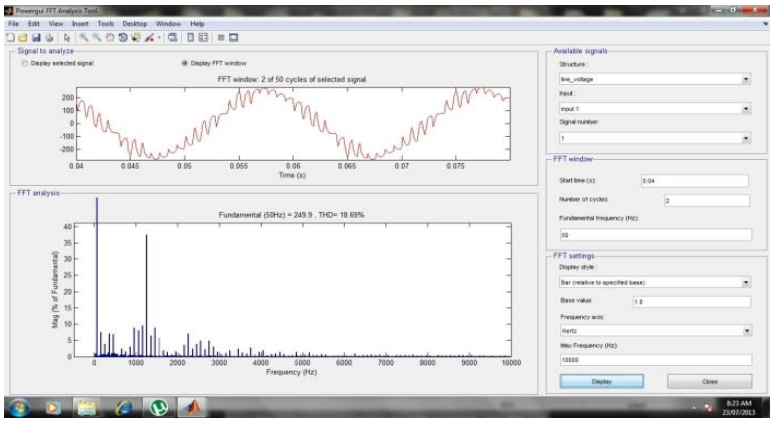

Fig. 15 Harmonic Spectrum of Three level diode clamped Inverter with filter of Phase Voltage at modulation Index=1

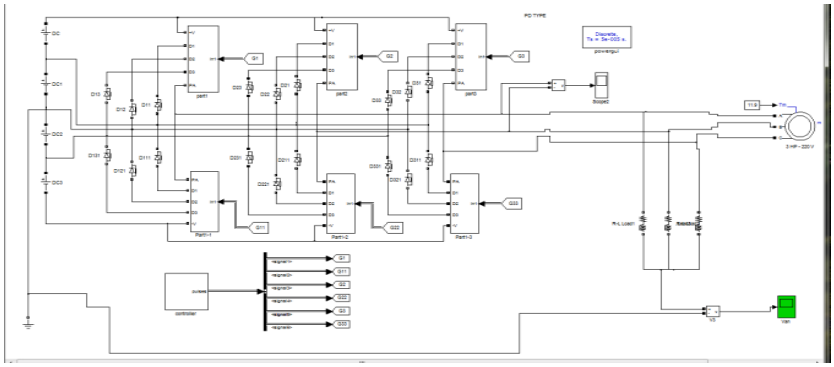

Fig. 16 Model of Five Level Diode Clamped Inverter fed Three Phase Induction Motor without filter

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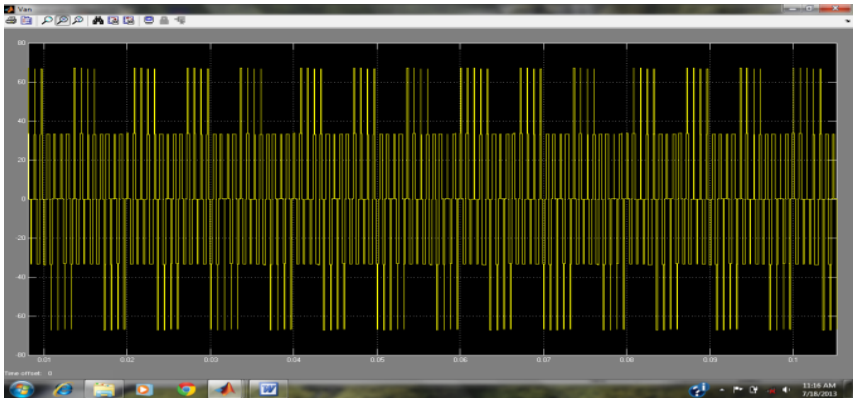

Fig. 17 CMV of Five Level Diode Clamped Inverter(PD PWM Technique) without filter

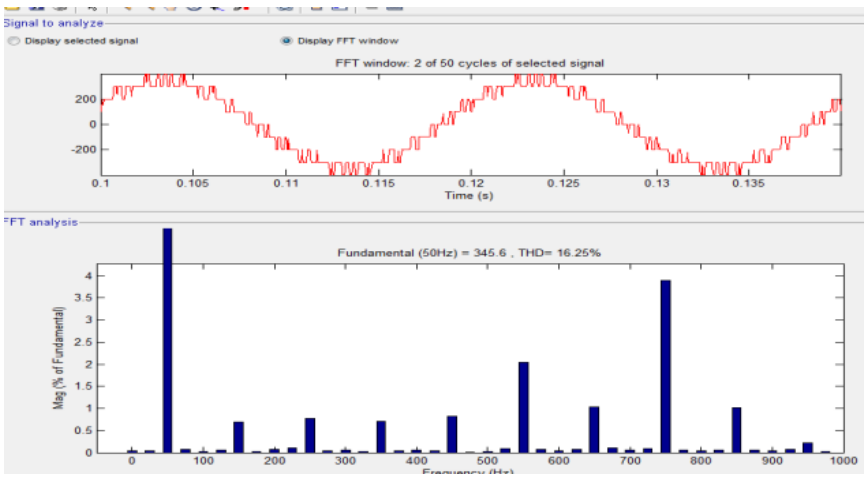

Fig. 18 Harmonic Spectrum of Five level diode clamped Inverter without filter Phase Voltage at modulation Index=1 (PD PWM Technique)

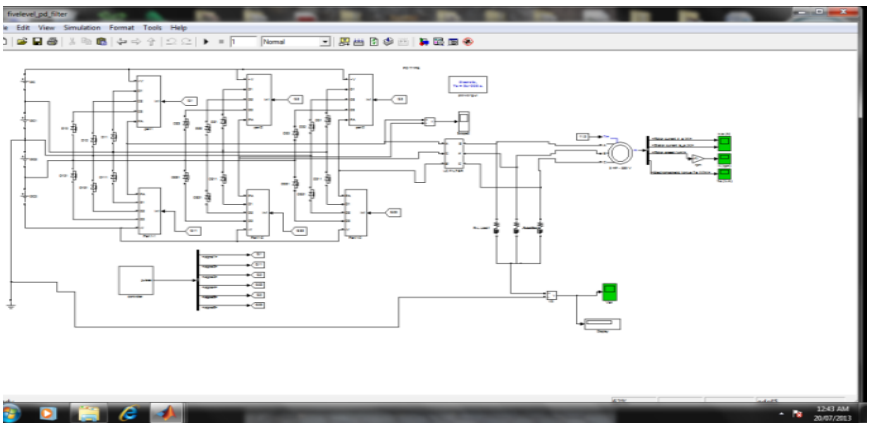

Fig. 19 Model of Five Level Diode Clamped Inverter fed Three Phase Induction Motor Drive with filter

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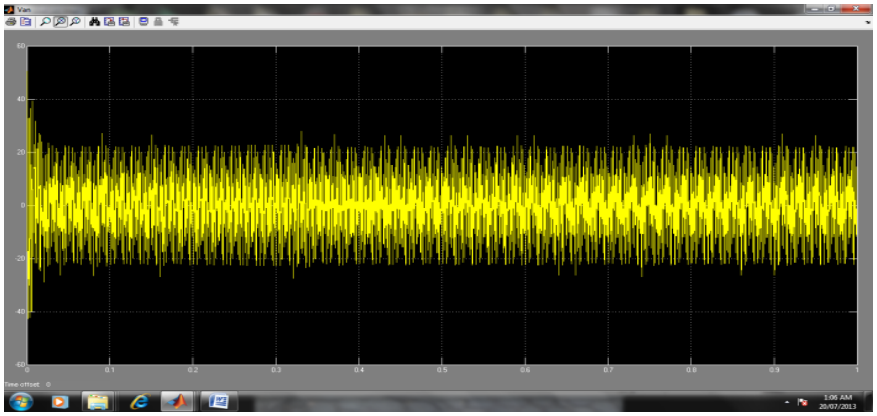

Fig. 20 CMV of Five Level Diode Clamped Inverter(PD PWM Technique) with filter

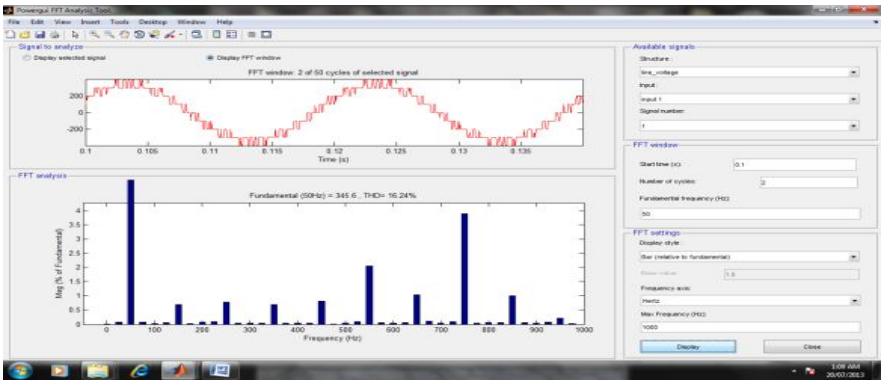

Fig. 21 Harmonic Spectrum of Five level diode clamped Inverter with filter Phase Voltage at modulation Index=1 (PD PWM Technique)

Table I Table Showing Comparison Of Thd For Different Levels

Diode Clamped Multilevel Inverter (PD PWM technique)	WithOut Filters		With Filters	
	CMV	THD %	CMV	THD %
Two Level	200	89.88 %	166.9	37.70 %
Three Level	66.67	31.86 %	7.721	18.69 %
Five Level	33.86	16.25 %	5..082	16.24

As per the Fig. s for the common mode voltage and the FFT Analysis window which have been shown above and refering Table I we can state that as the level increases the Common Mode Voltage as well as the Thermal Harmonic Distortion goes on decreasing and by applying the proposed filter to the two , three and five level model we were further able to reduce the corresponding Common mode voltage and the Thermal harmonic Distortion

VI. CONCLUSION

This paper has described the design and implementation of a passive filter . The purpose of the proposed filter is to eliminate both high-frequency common-mode and differential-mode voltage from the ac output voltage simultaneously. The output of proposed filter have been verified by simulation and experimental results carried out on 415V/3Hp motor system. Total Harmonic Distortion and Common mode voltage was evaluated for different levels. It is found that common mode voltage, differential mode voltage & harmonic distortion are less in multilevel inverter fed induction

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motor as compare to Conventional two level inverter. Size & rating of filter in two level inverter are large as compare to multilevel inverter. The energy consumed in multilevel inverter fed AC drive is less as compare to two level inverter.

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