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Modeling and Voltage Balance Control of MMLC Using PI Controller

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ABSTRACT: A modular multilevel converter (MMC) is one of the next generation multilevel converters intended for high- or medium-voltage power conversion without transformers. However, no paper has made an explicit discussion on voltage-balancing control. This paper deals with Multi Carrier pulse width-modulated modular multilevel converters (MCPWMMMCs) with focus on their circuit configurations and voltage balancing control. If the unbalanced load is connected with three phase system, the capacitor's charging and discharging will be affected so the proper output voltage can't be obtained. It must be adjusted as proper manner in terms of using PI controller as a compensator which gives proper output voltage and current. Thus the output voltage changes into the proper manner. MATLAB simulink environment is used to simulate the results.

INDEX TERMS: Modular Multilevel converters, voltage-balancing control, Multi Carrier Pulse Width Modulation.

I. INTRODUCTION

High-power converters for utility applications require line-frequency transformers for the purpose of enhancing their voltage or current rating [1]–[4]. The 80-MVA Static synchronous Compensator (STATCOM) commissioned in 2004 consists of 18 neutral-point-clamped (NPC) converter legs [4], where each of the ac sides is connected in series by the corresponding transformer. The use of line-frequency transformers, however, not only makes the converter heavy and bulky, but also induces the so-called dc magnetic flux deviation when a single-line-to-ground fault occurs [5]. Recently, many scientists and engineers of power systems and power electronics have been involved in multilevel converters intended for achieving medium-voltage power conversion without transformers [6]–[8]. Two of the representatives are:

1) The diode-clamped multilevel converter (DCMC) [6], [7];

2) The flying-capacitor multilevel converter (FCMC) [8].

The three-level DCMC or a NPC converter [9] has been put into practical use [10]. If a voltage-level number is more than three in the DCMC, inherent voltage imbalance occurs in the series-connected dc capacitors, thus resulting in requiring an external balancing circuit (such as a buck–boost chopper) for a pair of dc capacitors [11]. Furthermore, a significant increase in the clamping diodes required renders assembling and building of each leg more complex and difficult. Thus, a reasonable voltage-level number would be up to five from a practical point of view.

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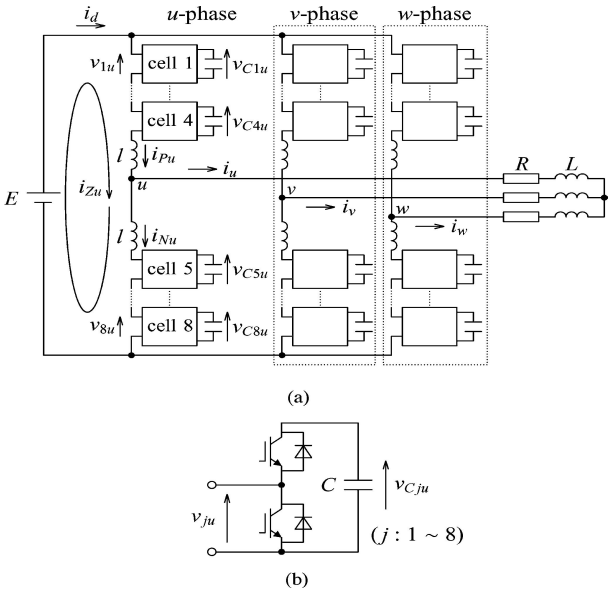

Fig.1. Circuit configuration of a chopper-cell-type modular multilevel inverter: (a) Power circuit and (b) Bidirectional PWM chopper-cell with a floating dc capacitor.

As for the FCMC, the four-level pulse width modulation (PWM) inverter is currently produced by one manufacture of industrial medium-voltage drives [12]. However, the high expense of flying capacitors at low carrier frequencies (say, lower than 1 kHz) is the major disadvantage of the FCMC [13].A modular multilevel converter (MMC) has been proposed in [14]–[20], intended for high-power applications. Fig. 1 shows a basic circuit configuration of a three-phase modular multilevel inverter.

Each leg consists of two stacks of multiple bidirectional cascaded chopper-cells and two non coupled buffer inductors. The MMC is suitable for high- or medium-voltage power conversion due to easy construction/assembling and flexibility in converter design. Siemens has a plan of putting it into practical use with the trade name of "high-voltage direct current (HVDC) - plus." It is reported in [19] that a system configuration of the HVDC-plus has a power rating of 400 MVA, a dc-link voltage of ±200 kV, and 200 cascaded chopper cells per leg. The authors of [14]–[20], however, have made no detailed description of staircase modulation, especially about a crucial issue of how to achieve voltage balancing of 200 floating dc capacitors per leg. Moreover, no experimental result has been reported yet.

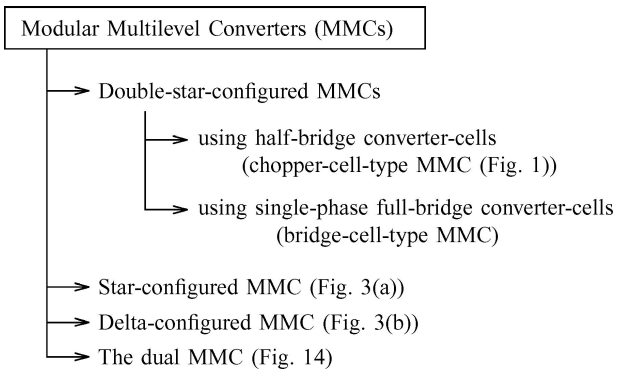

Fig.2. Classification of modular multilevel converters.

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This paper focuses on voltage-balancing control and operating performance of a pulse width-modulated MMC (PWMMMC) The final aim of this paper is to apply the PWM-MMC to medium-voltage power converters in a power rating of 1–10 MVA, a dc-link voltage of 10–30 kV, and a switching frequency of 200–2000 Hz. Balancing control enables achievement of voltage balancing of multiple floating dc capacitors without any external circuit. In addition, this paper proposes the closed loop connection of MMC for low-voltage large-current power conversion. Each dc side of positive and negative chopper-cells possesses a common dc capacitor, whereas its ac side is connected in parallel via multiple buffer inductors. The similarity between the two MMCs exists in terms of circuit configuration and control method.

II.TOPOLOGIES OF MMCS

A. *Classification from the Topologies*

Fig. 2 shows a classification of MMCs based on single-phase half-bridge or full-bridge converter-cells. From their topologies, MMCs can be classified into:

1) Double-star-configured MMCs;

2) A star-configured MMC [Fig. 3(a)];

3) A delta-configured MMC [Fig. 3(b)]; and

4) The dual MMC (Fig. 14).

Moreover, the double-star-configured MMCs can be classified into:

1) A chopper-cell-type MMC (Fig. 1); and

2) A bridge-cell-type MMC.

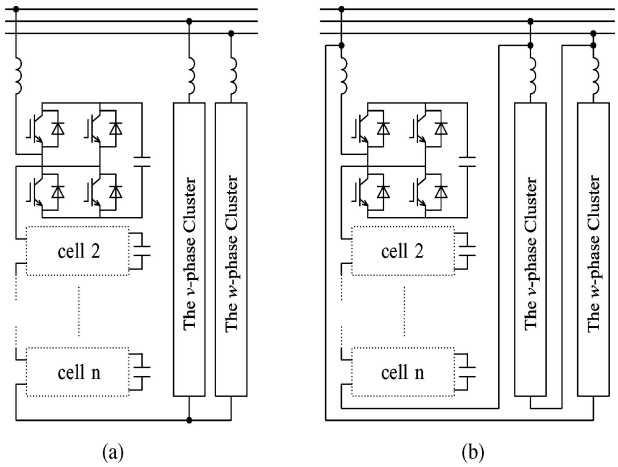

Fig.3. Circuit configuration of MMCs: (a) Star-configured MMC, and (b) Delta-configured MMC.

that the star/delta-configured MMC topology is not applicable to industrial motor drives, but it is suitable for STATCOMs and energy storage systems [21]–[23]. This consideration is one of the most significant differences in function and application between the double-star-configured MMC topology in Fig. 1 and the star/delta-configured MMC topology in Fig. 3.The bridge-cell-type MMC replaces the chopper cell in Fig. 1(b) with single-phase full-bridge

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converter cells. Hence, the dc-voltage source *E* can be replaced with a single-phase ac-voltage source [16]. The detail of the dual MMC is discussed in Section V. In this paper, the chopper-cell-type MMC is referred to simply as "the MMC" because attention is paid to it exclusively.

C. Definition of DC Loop Currents

Fig. 1 shows a three-phase inverter based on the MMC. Each leg of the circuit consists of two stacks of four bidirectional chopper-cells and two non coupled buffer inductors. Each chopper-cell consists of a floating dc capacitor and two insulated-gate bipolar transistors that form a bidirectional chopper. Attention is paid to the *u*-phase chopper-cells because the operating principle is identical among the three legs.

The following circuit equation exists in Fig. 1(a) 1:

$$E = \sum_{j=1}^{8} v_{ju} + l\frac{d}{dt}(i_{Pu} + i_{Nu})$$

Here, *E* is a supply dc voltage, *vju* is an output voltage of the *u* phase chopper-cell numbered *j*, *l* is a buffer inductance and *iPu* and *iNu* are positive- and negative-arm currents, respectively. The Kirchhoff's voltage law (KVL) loop given by (1) is referred to as the "dc loop," which is independent of the load. The circulating current along the *u*-phase dc loop, *iZu* can be defined as,

$$i_{Zu} = i_{Pu} - \frac{i_u}{2} = i_{Nu} + \frac{i_u}{2}$$

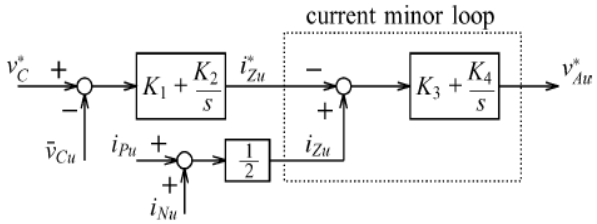

Fig.4. Block diagram of dc-capacitor voltage control: Averaging control.

Note that *iP u*, *iNu*, *iu*, and *id* are branch currents whereas *iZu* is a loop current that is impossible to measure directly.

III. CONTROL METHOD OF THE MMC

The voltage-balancing control of eight floating dc capacitors per leg in Fig. 1 can be explained by the following method.

A. Averaging Control

Fig. 4 shows a block diagram of the averaging control. It forces the *u*-phase average voltage $\bar{v}Cu$ to follow its command $v*C$, where $\bar{v}Cu$ is given by

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$$\bar{v}_{Cu} = \frac{1}{8}\sum_{j=1}^{8} v_{Cju}$$

Let a dc-loop current command of *iZu* be *i∗Zu*, as shown in Fig. 4. It is given by

$$i^*_{Zu} = K_1(v^*_C - \bar{v}_{Cu}) + K_2 \int (v^*_C - \bar{v}_{Cu})\, dt.$$

The voltage command obtained from the averaging control, *v∗Au* is given by

$$v^*_{Au} = K_3(i_{Zu} - i^*_{Zu}) + K_4 \int (i_{Zu} - i^*_{Zu})\, dt.$$

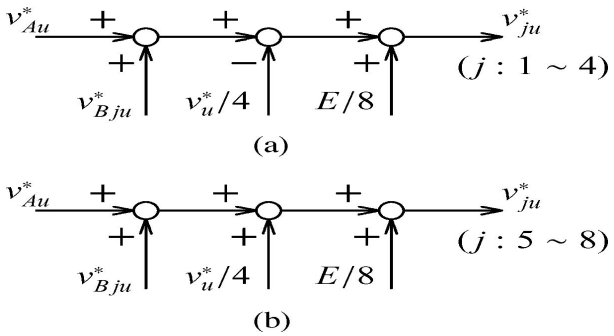

Fig.5. Voltage command of each arm: (a) Positive arm and (b) Negative arm.

active power should be taken from the dc power supply into the four chopper-cells. When *iP u* is positive, the product of *vBju* (= *v∗Bju*) and *iP u* forms the positive active power. When *iP u* is negative, the polarity of *vBju* should get inverse to take the positive active power. Finally, *v∗Bju* for *j* = 1− 4 is represented as,

$$v^*_{Bju} = \begin{cases} K_5(v^*_C - v_{Cju}) & (i_{Pu} > 0) \\ -K_5(v^*_C - v_{Cju}) & (i_{Pu} < 0) \end{cases}$$

While *v∗Bju* for *j* = 5− 8 is also represented as,

$$v^*_{Bju} = \begin{cases} K_5(v^*_C - v_{Cju}) & (i_{Nu} > 0) \\ -K_5(v^*_C - v_{Cju}) & (i_{Nu} < 0). \end{cases}$$

Fig. 5 shows a voltage command of each chopper-cell *v∗ju*. The positive-arm and negative-arm commands are obtained.

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$$v_{ju}^{*} = v_{Au}^{*} + v_{Bju}^{*} - \frac{v_{u}^{*}}{4} + \frac{E}{8} \quad (j:1-4)$$

$$v_{ju}^{*} = v_{Au}^{*} + v_{Bju}^{*} + \frac{v_{u}^{*}}{4} + \frac{E}{8} \quad (j:5-8)$$

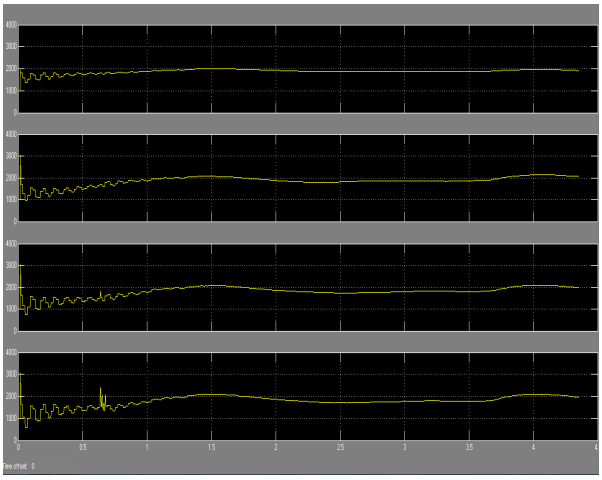
where $v*u$ is an ac-voltage command for the u-phase load. Note that Fig. 5 includes the feed forward control of the dc supply voltage E. The voltage command $v*ju$ is normalized by each dc-capacitor voltage $vCju$, followed by comparison with a triangular waveform having a maximal value of unity and a minimal value of zero with a carrier frequency of fC. The actual switching frequency of each chopper-cell, fS is equal to fC. The eight chopper-cells have the eight triangular waveforms with the same frequency but a phase difference of 45◦ (= 360◦/8) to each other for achieving harmonic cancellation and enhancing current controllability.

B. ***Simulated Results***

Fig. 6 shows simulated waveforms from Fig. 1. Tables I and II summarize circuit parameters and control gains used for simulation using a software package of the "PSCAD/EMTDC" [24]. The dc supply voltage E and the rated active power P are set as E = 9 kV and P = 1 MW, and therefore, the nominal rated line-to-line rms voltage of the MMC is 5.5 kV. An intrinsic one-sampling delay occurs due to digital control. The dc capacitor voltage command of each chopper-cell is $v*C$ =2.25 kV while three-phase load voltage commands of each phase are given as

$$\begin{aligned} v_{u}^{*} &= 0.5E\sin 2\pi ft \\ v_{v}^{*} &= 0.5E\sin\left(2\pi ft - \frac{2}{3}\pi\right) \\ v_{w}^{*} &= 0.5E\sin\left(2\pi ft - \frac{4}{3}\pi\right) \\ E &= 9\ \mathrm{kV} \\ f &= 50\ \mathrm{Hz}. \end{aligned}$$

Capacitor Voltage Balancing Output



Three phase output voltage

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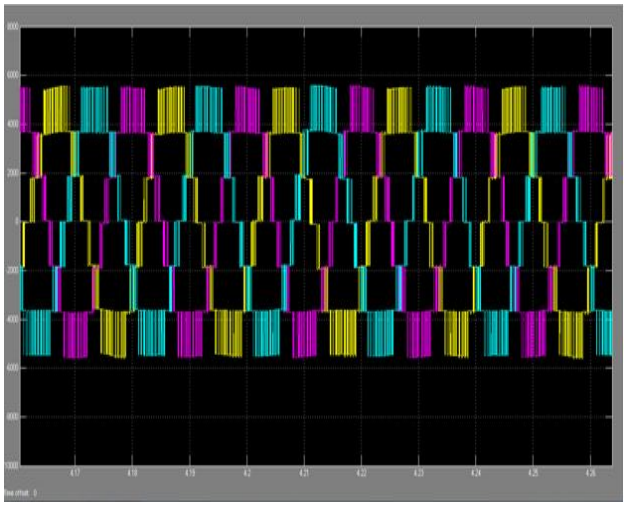

Three phase output current

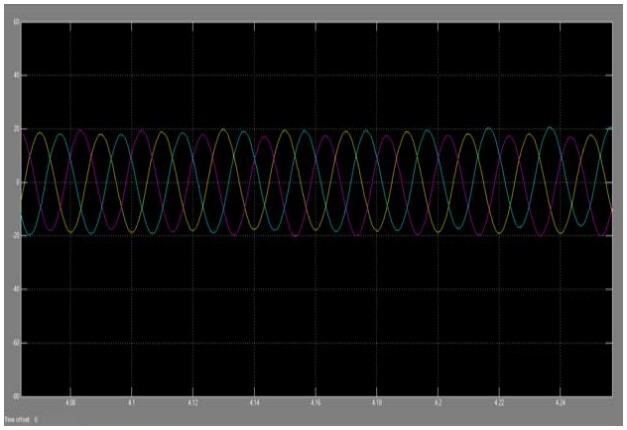

Fig.6. Simulated waveforms obtained from Fig. 1, where *f* = 50 Hz, *v∗C* =2.25 kV, and *E* = 9 kV.

Note that *v∗u*, *v∗v*, and *v∗w* are the three-phase line-to-neutral voltages. In Fig. 6, each chopper cell is operated at unity modulation index. In Table I, a unit capacitance constant *H* is defined as,

$$H = \frac{3 \times 8 \times \frac{1}{2} C V_C^2}{P}$$
$$= \frac{12 \times 1.9 \times 10^{-3} \times 2.25^2 \times 10^6}{10^6} = 0.115$$

where *VC* is the rated dc voltage of each chopper cell. Note that *H* is defined as a ratio of all electrostatic energy stored in dc capacitors with respect to rated active power [25]. Therefore, *H* has a unit of second.2 Fig. 6 indicates that *vuv* is a 17-level line-to-line voltage, achieving voltage balancing of all the dc capacitors. The dc input power *pd* is represented as

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$$p_d = E \times i_d$$

where *id* is a dc input current. The waveform of *pd* includes the following two frequency components: one is a 6th-frequency (300 Hz) component stemming from a three-phase full-bridge converter, and the other is a fundamental frequency (50 Hz) component stemming from an output frequency of 50 Hz. The detailed analysis of each waveform will be carried out in the next section.

TABLE I

CIRCUIT PARAMETERS USED FOR SIMULATION

Rated active power	P	1 MW
Rated line-to-line rms voltage	V	5.5 kV
Rated rms current	I	105 A
Rated frequency	f	50 Hz
DC supply voltage	E	9 kV
Buffer inductance	l	3 mH (3.1%)
DC capacitance	C	1.9 mF
DC capacitor voltage	V_C	2.25 kV (= 9 kV/4)
Unit capacitance constant [25]	H	115 ms
Carrier frequency	f_C	2 kHz
Equivalent switching frequency	$8f_C$	16 kHz
Load power factor	$\cos\phi$	≃ 0.9 at 50 Hz
Load inductance	L	6 mH (6.2%)

Values in () are on a three-phase 5.5-kV, 1-MW, and 50-Hz base.

Fig. 6. Simulated waveforms obtained from Fig. 1, where f = 50 Hz, v∗C =2.25 kV, and E = 9 kV.

TABLE II

CONTROL GAINS USED FOR SIMULATION

Proportional gain of averaging control	K_1	0.5 A/V
Integral gain of averaging control	K_2	150 A/(V·s)
Proportional gain of current control	K_3	1.5 V/A
Integral gain of current control	K_4	150 V/(A·s)
Proportional gain of balancing control	K_5	0.35

V. CONCLUSION

This paper has dealt with the balancing of Multi Carrier PWM-MMCs, proposing their control method and verifying their operating principle. Computer simulation using the "PSCAD/EMTDC" software package has confirmed the proper operation of the three-phase Multi Carrier PWM-MMC. The MMC is showing considerable promise as a power converter for medium-voltage motor-drives, high-voltage direct current (HVDC) systems, STATCOMs, and back-to-back systems. Thus the output voltages are balanced even though unbalanced load is connected to the three phase system.

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