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Low Power UWB Weak-Inversion Mixer for RF Transceiver

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ABSTRACT: A low power ultra wide band down conversion mixer is presented briefly in this paper. In this design, transistors are biased to operate in weak-inversion region so as to reduce the total power consumption of the mixers. The proposed circuit uses source-driven topology and has been designed using 0.18µm standard RF CMOS process. The simulated result shows a total power consumption of 1mW. In addition, under 2V power supply, the proposed mixer gives conversion gain of 21 dB from 1 GHz to 10 GHz, noise figure of 14 dB, OIP3 of -46.9 dBm, IIP3 of 27.7 dBm and 1dB compression gain of -6dBm.

KEYWORDS: Low power mixer, double balanced, weak inversion mixer, source driven.

I.INTRODUCTION

The radio frequency (RF) circuit design is currently enjoying a revolution, and explosive growth in wireless telecommunications. One of the most important components of the RF front-end architecture is the down-conversion mixer, which is used to translate RF signal into baseband signal. The low-power down-conversion mixers designs are crucial for wireless transceivers to enhance the receiver performance. It can be realized by various methods, such as the CMOS passive and active mixers. The CMOS passive mixers, with advantages of high linearity and zero dc power consumption, but they suffer from the design challenge of high conversion loss and high local oscillator (LO) power. Therefore, mixers utilizing passive topologies are difficult to be integrated into an ultra-low-power system, due to the power-hungry LO buffer or even a power amplifier as a LO driver. In contrast with passive mixers, the CMOS active mixers have the advantages of low conversion loss and low LO power requirements. Although these active mixers exhibit good RF performance, the dc power consumption cannot be neglected from the system power budget. Different kind of advanced technology mixers, based on the CMOS process, have been reported [1]–[8]. One of the most popular is the Gilbert-type mixer, which has high even-order linearity and a good port-to-port isolation to release the dc offset problem [2]. However, it does have drawbacks, such as relatively high supply voltage and power consumption due to a number of stacked transistors operating in the saturation region. The folded structure mixer operates at a low supply voltage [4] due to the small number of stacked transistors; however, as the folded structure requires a higher dc current, it has similar power consumption compared to the Gilbert-type mixer. The current bleeding technique was designed to improve the mixer noise since less current flows at the LO switching stage [6]. However, the parasitic capacitance increases between the LO switching stage, the RF transconductance stage, and the current bleeding circuit. To eliminate this parasitic capacitance, resonating inductors could be used, though the chip size would increase while the bandwidth would decrease [8].

This paper presents a double-balanced source-driven mixer using bulk-injection technique. The proposed source-driven mixer consumes only a few watts of dc power consumption, accomplished by the mixer core in the weak inversion biasing region while maintaining reasonable RF performance. The Gilbert-type mixer has the drawback of parasitic capacitance between the RF and LO stages giving rise to a lower conversion gain at a high frequency; this results from the RF current leaking to the shunt parasitic capacitance. However, the source-driven topology used in this study has merit in that the integration of the RF and LO stages into a single transistor eliminates any interconnecting parasitic capacitance. In source-driven topology, the received RF signal is applied to gate of the transistor and the LO signal is applied to the source of the transistor.

II. OPERATION PRINCIPLE OF PROPOSED MIXER CIRCUIT

The figure1 shows the working principle of proposed down conversion mixer. It shows that when incoming RF signal is applied to the gate and LO signal is applied to the source terminal of the mosfet, IF signal is obtained at the drain

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terminal which is the product of RF and LO signal. When the LO signal varies, the drain to source voltage of the mosfet changes hence the mosfet will move to weak-inversion region. Thus, in this design LO signal controls the mixing operation of the circuit. The proper LO switching in the mixer makes the mosfet to operate in weak-inversion region. During when mosfet operate in weak inversion region, the drain current Ids of the mosfet decreases, hence the total dc bias current flowing in the circuit decreases. Since the power consumption is directly proportional to dc bias current, the total power consumed will get reduced.

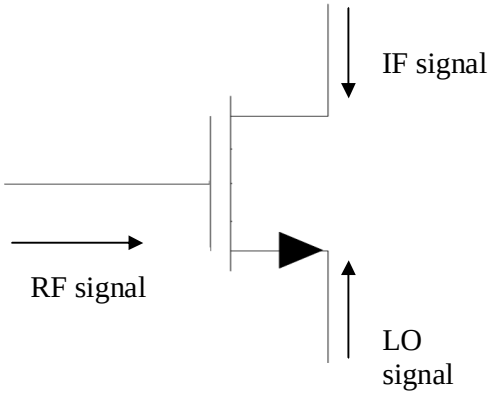

Fig. 1 working principle of proposed mixer

In the weak inversion region, the gate to source voltage Vgs is less than the threshold voltage Vth of the mosfet. Then the drain current Ids is given by,

$$Ids = \frac{W}{L} Ioexp(\frac{Vgs}{\eta VT}) \quad \ldots (1)$$

Where η is the weak-inversion slope factor (1< η < 3), Io is process dependent parameter which depend on Vth, W is the width of the mosfet, L is the effective gate length of the mosfet and VT is the thermal voltage which is equal to 0.025V. Also, the transconductance of the transistor is given by

$$gm = \frac{Ids}{\eta VT} \quad \ldots (2)$$

When the mosfet is driven in the weak inversion region the characteristic plot between the drain current Ids and the gate to source voltage Vgs will be exponential. If the mosfet is operated in strong inversion region the characteristic plot between Ids and Vgs will be having square-law characteristics.

III. PROPOSED WEAK-INVERSION SOURCE DRIVEN MIXER

The mixer is designed and simulated in gpdk 180nm technology. For improving the linearity by removing second order harmonics, a double-balanced topology is adopted in the proposed design. The complete schematic circuit is shown in fig. 2.

The frequency translation of the double-balanced mixer is provided by the commutating stage, M1–M4. The gate voltage of the mixer quad core (NM1–NM4) is biased at 0.7 V, which is smaller than the threshold voltage of approximately 1V in the gpdk 180-nm CMOS process. The mixer active loads, PM1 and PM2, with high output impedance can achieve high CG and further reduce the ac current flow through the mixer core. Two identical R guarantee the same common-mode dc voltage for the differential outputs of the mixer core.

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For ultra-low-power consumption and ultra-low LO power, a source-driven technique and a weak-inversion biasing technique are incorporated into the double-balance mixer design, where the RF and LO signals are applied to the gate and source of NM1–NM4, respectively, while the IF output signal is from the drain, as shown in Fig. 2. The mixer switching core, NM1–NM4, is biased at the weak-inversion region. For the transistor NM1 and NM4 differential input signal RF plus and RF minus, also at transistor NM2 and NM3 LO plus and LO minus are given respectively. A dc voltage is applied to the bulk terminal in order to increase the threshold voltage high so as to make the transistor operate in weak-inversion region. The differential output IF plus and IF minus is the required mixer output. The two resistors R determine the conversion of the mixer.

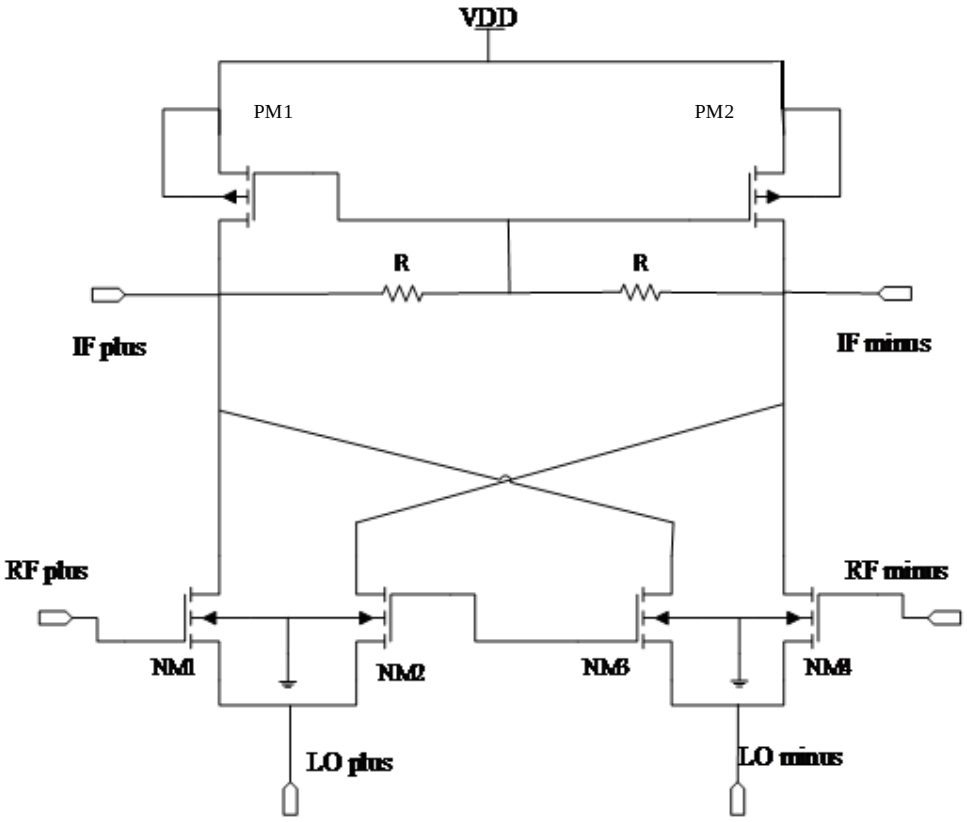

Fig.2 Schematic diagram of proposed weak-inversion source driven mixer

$$Conversion\ Gain(CG) = Constant * VLO^2 \quad \text{... (3)}$$

The above equation shows that Conversion Gain (CG) is proportional to Local Oscillator Voltage (VLO). In order to achieve ultra-low LO power, transconductance of the transistor must be large enough to provide the required CG of the mixer. However, a large transconductance is accompanied with a high drain–source current, Ids. On the other hand, in order to accomplish ultra-low power consumption, the drain–source current, Ids, of an NMOS transistor must be small enough, which leads to small transconductance and results in a low CG. Hence, a trade-off is involved among LO power, power consumption, and CG to choose an appropriate transconductance for circuit implementations. To achieve a given transconductance, the larger transistor size is accompanied with the smaller gate–source voltage (Vgs) and vice versa. The small signal drain current ids of the switch stage transistor around the quiescent bias point can be expressed by a Taylor- series expansion given below,

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Vol. 3, Issue 3, March 2014

$$ids = gm(vgs) + gm2\frac{Vgs^2}{1} + gm3\frac{Vgs^3}{1} + \cdots \quad \text{... (4)}$$

Where *gmi* represents the *i*th-order transconductance coefficients and Vgs represents the small-signal gate to source voltage. The third-order term *gm3* in (4) is the main contribution of harmful IM3 for RF systems.

IV.RESULTS AND DISCUSSIONS

A. *Conversion Gain vs. Local Oscillator Power*

After simulating the schematic design as shown in figure with input RF signal power of -20 dBm at RF frequency 5 GHz, the plot between Conversion Gain (CG) vs. LO power is shown in fig. 3.

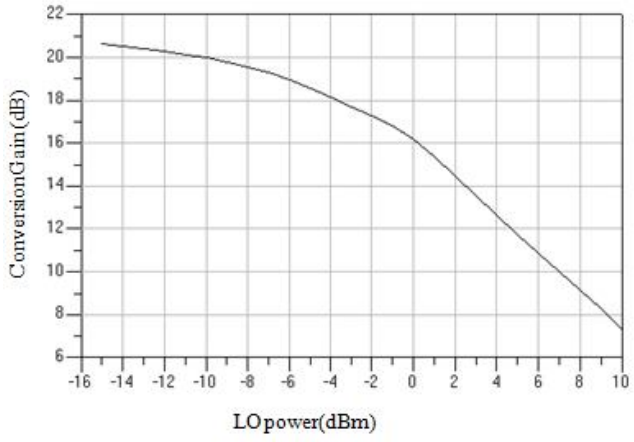

Fig.3 Conversion Gain of mixer with respect to LO power

The fig. 3 shows that when LO power is increased the conversion gain of the mixer decreases. The maximum conversion gain of 21 dB is achieved at LO power of 21dBm.

B. *Conversion Gain vs. RF frequency*

The above fig. 4 shows the plot between conversion gain and RF frequency. The input RF frequency is varied from 4GHz to 10GHz and a conversion gain of 21 dB is obtained at 5GHz.

C. *Noise Figure vs. Local Oscillator Power*

The fig. 5 shows the plot between Noise Figure (NF) and LO power. From the plot it is clear that the noise figure decreases as the power of the LO signal increases. From the above figure4 it is clear that a high noise added when the LO Power is made lesser than -30dBm. A noise figure of 14dB is obtained when the power of the LO signal is increased beyond -25 dBm. Since in the proposed system LO signal is applied to the source terminal during the negative excursion of the voltage of LO, the Vds increases hence conversion gain increases.

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Vol. 3, Issue 3, March 2014

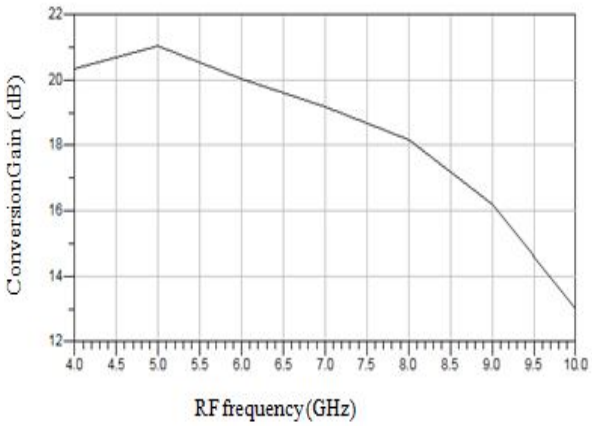

Fig. 4 Conversion Gain vs. RF frequency

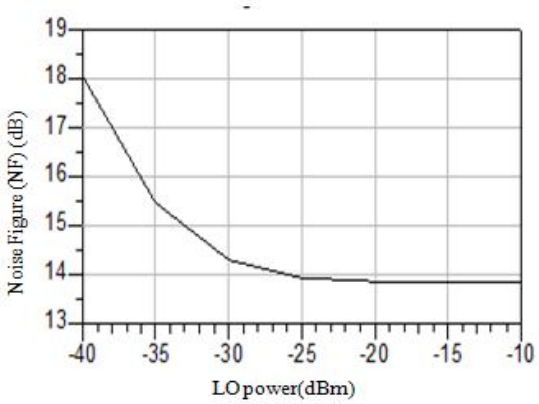

Fig. 5 Noise Figure vs. LO power

D. *Power Consumption of the proposed mixer*

The fig. 6 shows the instantaneous current flowing through the circuit. The power consumption is calculated by multiplying average current and dc voltage. The calculated power consumption for a 2V supply voltage is 1mW.

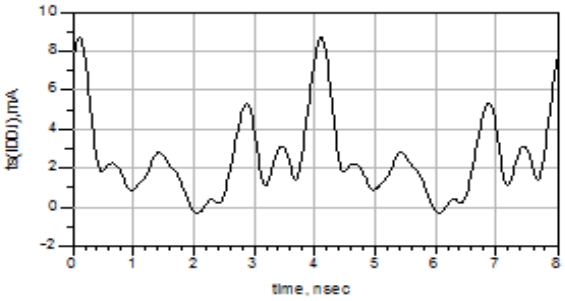

Fig. 6 Instantaneous current

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E. *1-dB Gain Compression Point*

1-dB compression point is the input signal level that causes output signal to drop by 1dB. Compression of gain is caused by non-linear characteristics of the device when run at high levels. With any signal, as the input level is increased beyond the linear range, gain compression will occur. The non-linear characteristics of the device are mainly due the presence of harmonics mainly third-order harmonics. The component of third-order harmonics is having opposite sign that of the fundamental component, thus when input signal is increased; the third-order component will suppress the overall gain.

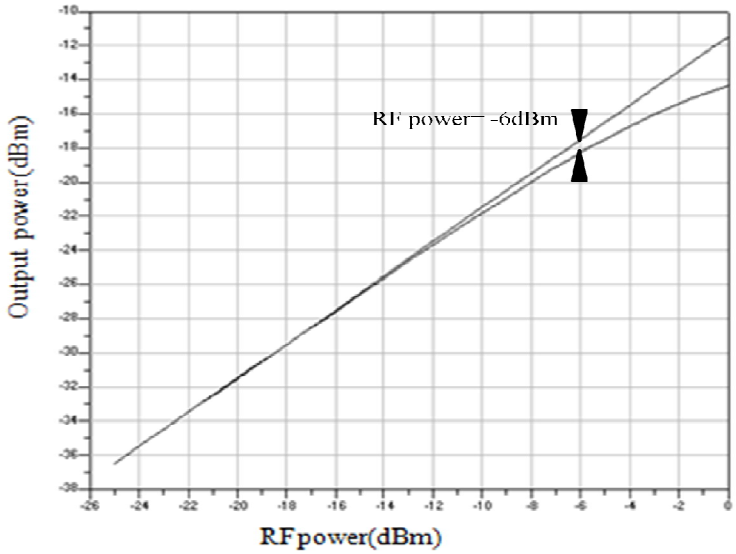

Fig. 7 1-dB gain compression

The above fig. 7 shows that gain compression of 1-dB occurs when input power reaches -6dBm (0.251mW) or at 0.312 Vpp.

F. Intermodulation Distortion

If two interferers are applied to a nonlinear system, the output generally exhibits component that are not harmonics of these frequencies. This leads to a phenomena called Intermodulation.

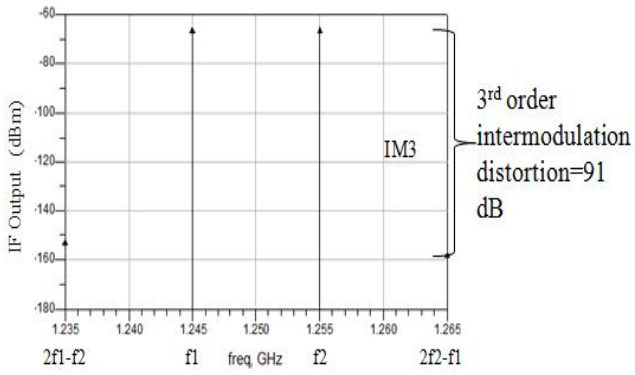

Fig .8 Intermodulation distortions

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A two tone test is adopted here to find the intermodulation. From the Fig. 8 two fundamental tones are applied having frequencies 1.245 GHz and 1.255 GHz which is represented by f1 and f2 respectively. Thus 2f1-f2 at 1.235 GHz and 2f2-f1 at 1.265 GHz are the third-order components. The third-order intermodulation distortion obtained through simulation is 91 dB.

G. *Third-Order Intercept Point*

If the amplitude of each fundamental tone is increased, the amplitude of third-order harmonic component increases three times more. If the amplitude is continuously increased, the amplitude of Inter Modulation (IM) becomes equal to that of the fundamental tone. The simulated result represented by Fig.9 shows that the proposed mixer is having Input Intercept Point (IIP3) as 27.7 dBm and Output Intercept Point (OIP3) as -46.9 dBm.

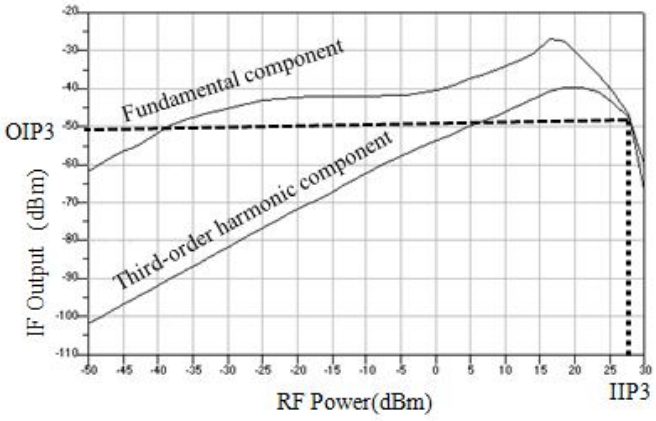

Fig. 9 Third-Order Intercept Point

TABLE I
TRANSISTOR ASPECT RATIO

Transistor	W/L (µm/µm)
NM1 to NM4	2/0.18
PM1 to PM12	4/0.18

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TABLE II
COMPARISON WITH OTHER MIXER TOPOLOGY

Reference	Frequency (GHz)	Power Consumption (mW)	NF (dB)	Conversion Gain (dB)	IIP3 (dBm)	Process
[1] 2012	0.5-6	0.28	15.2	6	0	180 nm
[3] 2012	0.5-3	5.4	16.5	2.2	10	180 nm
[5] 2012	2.4-11.9	0.88	11.7	7.6 to 9.9	-10 to -15.5	180 nm
[7] 2013	53-70	0.453	18	5.9±1.5	-4	90 nm
[9] 2010	1-10.5	5m	7.6	12.8	-	65 nm
[10] 2012	21-29	39.5	4.6±0.5	23.7±1.4	-	180 nm
[11] 2012	5	21	10.6	12	-12	90 nm
This Work 2014	**1-10**	**1**	**14**	**21**	**27.7**	**180 nm**

Table II shows the comparison of different topology with this work.

V. CONCLUSION

This paper presents a low power double-balanced weak-inversion down conversion mixer using source driven topology. The mixer is designed using 180nm CMOS process. The simulated result shows the Conversion Gain (CG) of 21 dB from 1GHz to 10 GHz and Noise Figure (NF) of 14 dB. The mixer consumes only 1mW of power and Input Intercept Point (IIP3) at 27.7 dBm. The designed mixer can be used in receiver front-end of Ultra-Wide Band (UWB) applications.

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Vol. 3, Issue 3, March 2014

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BIOGRAPHY

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