



Implementation of New Multilevel Inverter Using Minimum Number of Components

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ABSTRACT: Multilevel inverter is used to synthesize a near sinusoidal voltage. Power quality is improved with the increase in number of levels. However, the number of switching devices and other components increase which would result in increase in cost and control complexity. To alleviate this problem, a multilevel inverter of hundred and twenty seven (127) levels with only ten switches and six diodes is proposed. The system uses a bypass diode technique with only one H-bridge for any levels. Simulation is carried out in Matlab for 127 levels and the output is figured out. The same set up is realized for seven (7) levels with the hardware components and the output is verified. The system yields better results when compared to earlier works with reduced control circuit complexity and cost. Further, the suggested topology reduces the number of DC sources, switches and power diodes.

KEYWORDS: MOSFET, IGBT, Cascaded Multilevel Inverter, H-Bridge Multilevel Inverter, Battery, Diode.

I. INTRODUCTION

Three basic multilevel inverter topologies are the Neutral Point Clamped (NPC) or diode clamped, the flying capacitor (FC) or capacitor clamped and the cascaded H-bridge [1]. The drawbacks of NPC topology are unequal voltage sharing among series connected capacitor that result dc-link capacitors are unbalanced and requiring a great number of clamping diodes for higher level. The FC as clamping devices has several attractive properties when compared with NPC [1]-[5]. The advantage of this transformer less operation. It can be classified into two types namely single source and multi-source multilevel inverter. Single source system has only one DC source [8]. In single source system the remaining are clamping diodes or capacitors. It is classified into two types namely diode clamped multilevel inverter and flying capacitor multilevel inverter [1]-[9]. The main disadvantage of flying capacitor inverter is that it requires large number of capacitors. Diode clamped inverter restricts the use of high power range of operations [4]-[6]. The shortcomings in single source systems are overcome by introducing a multisource multilevel inverter.

In multi-source inverter system has two or more DC sources and it is a series power cells. It classified into two types namely cascaded H-Bridge multilevel inverter and Hybrid H-Bridge multilevel inverter. H-Bridge multilevel inverter can be easily scaled to the power levels [7]. However, it requires large number of semiconductor switches [1]-[7]. Multilevel inverter has gained more attention for high power application in recent years which can operate at high switching frequencies while producing low order harmonic components [1]. This inverter not only achieves the high power ratings but also enables the use of renewable energy sources such as photovoltaic, wind and fuel cells that can be easily interfaced to a multilevel inverter. For a medium voltage grid, it is connected to one power semiconductor switch directly [1]-[2]. In multilevel inverter, the power quality is improved as the number of levels increases at the output voltage [3]. The number of switching devices and other components increases along with the cost and complexity of the control circuit and thereby reducing the overall reliability and efficiency of the inverter.

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II. SYSTEM MODEL

A new basic multilevel module (MLM) for the multilevel converter has been proposed. The proposed topology is a combination of MLMs and full-bridges converter. The proposed topology extends the design flexibility and the possibilities to optimize the converter for various objectives. It has been shown that the structure, consisting of MLMs with two switches has the minimum number of switches for a given number of voltage level. The proposed multilevel inverter has a general structure of the hybrid multilevel inverter as shown in Fig 1. Each stage has separate voltage source (V_{dc1} , V_{dc2} , and V_{dc3}) connected in cascade. Only One H Bridge is required for the single phase system along with a switch and a diode for each voltage source. In the conventional method, twenty one (21) switches are used to obtain hundred and twenty five (125) levels. Due to twenty one switches, the harmonics, switching losses, cost and the total harmonic distortion are increased. This proposed topology increases the level to 127 with only 10 switches and six diodes. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to multilevel inverter system for a high power application.

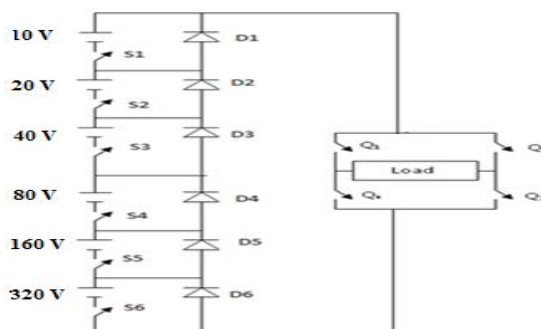


Fig 1. Circuit Diagram of Proposed Multilevel Inverter

III. PRINCIPLE OF OPERATION

The basic operation of the proposed system is to turn on s_1 and turn off s_2 and s_3 . The Output voltage is +1v. When the Switch s_2 is on and turn off s_1 and s_3 . The output voltage is +2v. The switch s_3 is on switch s_1 and s_2 are turn off. Similarly all the combinations of switching states are turn on and off with respect to the driver circuit. Only one H-bridge is required for get the both positive and negative output voltage levels of the system. The advantage of modified system increases the level with low number of switches.

The S number of DC sources or stages are calculated by using the equation,

$$N_{\text{level}} = 2^{s+1} - 1 \quad (1)$$

The voltage on each stage can be calculated by using the equation,

$$V_{\text{out}} = 2^{s-1} V_{\text{in}} \quad (2)$$

The number of switches used in the topology is given by the equation,

$$N_{\text{switch}} = S + 4 \quad (3)$$

IV. SIMULATION SETUP

The optimal multilevel structure with minimum used gate driver circuits based on the topology proposed is simulated using Matlab. The proposed system with 10 switches and 6 diodes is simulated for 127 levels for 1V. The output of pulse repeater is given to the switching devices (IGBT). The switching pulse amplitude is 1V. The control voltages for switching devices S1, S2 and S3 and for inverter switches Q1, Q2, Q3 and Q4 is through gate triggering circuits shown in Fig 2. For validating the results, the existing system with 21 switches.e .Three legs each with 7 switches is also simulated. The reason for increased number of switches in the existing system is that each leg has separate H-bridge. To overwhelm this drawback, the proposed system uses only one H-Bridge for any levels. The efficiency of the proposed system is high when compared to existing method since the output waveform is sinusoidal with reduced lower order harmonics.

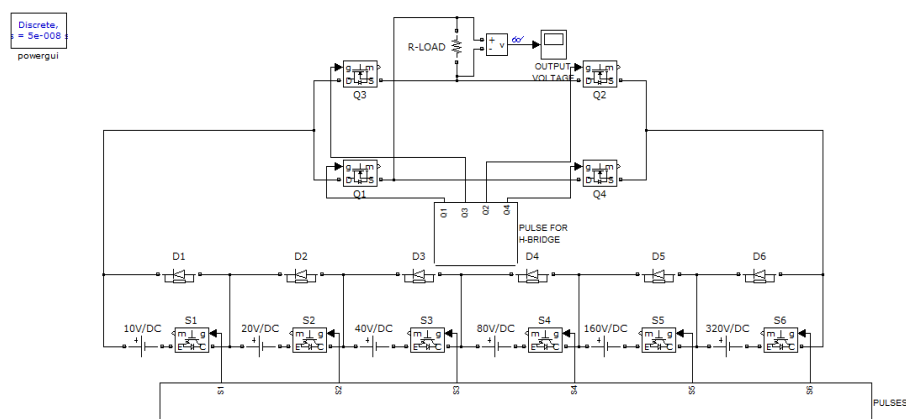


Fig 2.Simulation Diagram of Proposed System

IV.HARDWARE DESIGN

The inverter is realized in hardware with seven switches and three diodes. The PIC microcontroller is used for generating control pulses. The hardware is have PIC 16F877A microcontroller. The DC supply given to sub inverters and the gating pulses are generated using microcontroller to the driver circuit and from the driver circuit the pulses are driven into the sub inverter circuit.

The hardware circuit consists of the following.

1. power supply
2. driver circuit
3. micro controller

A steady state dc voltage is obtained by rectifying the ac voltage, then filtering to a dc level, and finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies, or the output load connected to the dc voltage changes. A power supply can be built using a transformer connected to the ac supply line to step the ac voltage to a desired amplitude, then rectifying that ac voltage, filtering with a capacitor and RC filter, if desired, and finally regulating the dc voltage using an IC regulator. Microcontroller is a general purpose device, which integrates a number of the components of a microprocessor system on to single chip. It has inbuilt CPU, memory and peripherals to make it as a mini computer. A microcontroller contains the following.

1. The CPU core

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2. Memory(both ROM and RAM)
3. Some parallel digital i/o Microcontrollers will combine other devices such as:
4. A timer module to allow the microcontroller to perform tasks for certain time periods.
5. A serial i/o port to allow data to flow between the controller and other devices such as a PIC or another microcontroller.
6. An ADC to allow the microcontroller to accept analogue input data for processing.

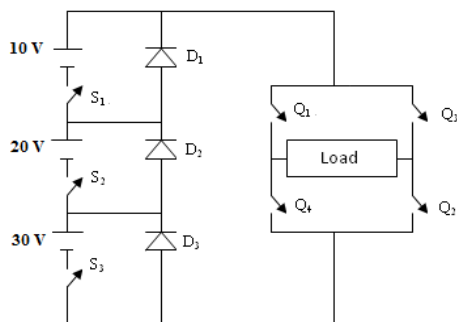


Fig 3. Hardware Circuit Diagram of New Multilevel inverter

Table 1. Switching States of New multilevel System

S.NO	STAGES	SWITCHING STATES		CURRENT PATH	VOLT IN DC
		ON	OFF		
1	I	S1	S2,S3	S1,D2,D3	1 V DC
2	II	S2	S1,S3	S1,D1,D3	2 V DC
3	III	S3	S1,S2	S3,D2,D1	3 V DC
4	IV	S1,S2	S3	S1,S2,D3	4 V DC
5	V	S2,S3	S1	S2,S3,D1	5 V DC
6	VI	S3,S1	S2	S1,S3,D2	6 V DC
7	VII	S1,S2,S3	-	S1,S2,S3	7 V DC
8	VIII	-	S1,S2,S3	D1,D2,D3	0 V

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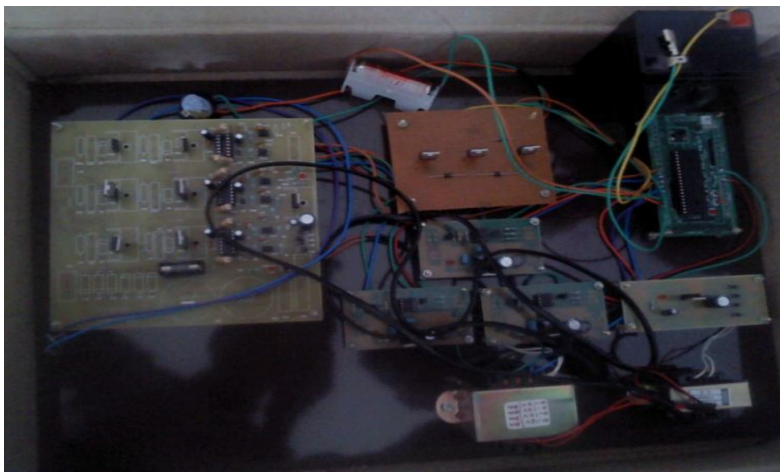


Fig 4.Photo copy of Hardware

VI. RESULTS AND DISCUSSION

The structure of optimal multilevel with minimum used switches with minimum driver circuits is simulated using Matlab. The same scenario is realized through hardware. For comparing the results, the existing system with 21 switches is also simulated. The lower order harmonics of the proposed system is significantly reduced. Hence it is inferred that the proposed system results are better when compared to existing system with reduced number of switches. The same results are observed when the setup is implemented in hardware. The efficiency of multilevel inverter predominates the existing with reduced Total Harmonic Distortion and switching losses.

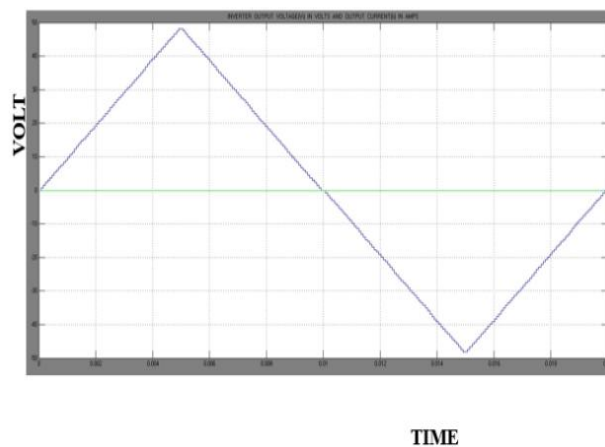


Fig 4.Simulation Output of New Multilevel System
(Output Level is 127)



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VII.CONCLUSION

Power quality is improved with the increase in number of levels of multilevel inverter. The number of switching devices and other components ultimately increase the cost and control complexity. Hence, a multilevel inverter of 127 levels with only ten switches and six diodes is proposed. The system uses a bypass diode technique with only one H-bridge for any levels. Simulation is carried out in Matlab and the experiment is carried out in hardware. The results are promising since the total harmonics distortion of proposed method is dramatically reduced with reduced switches, switching losses, cost, and low order harmonics with improved efficiency.

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