



High Speed Multioutput 128bit Carry- Lookahead Adders Using Domino Logic

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ABSTRACT: Addition is the fundamental operation for any VLSI processors or digital signal processing. In this paper focuses on carry -look ahead adders have done research on the design of high-speed, low-area, or low-power adders. Here domino logic is used for implementation and simulation of 128 bit Carry- look ahead adder based HSPICE Tool. In adder circuits propagation delay is the main drawback. To overcome this drawback the domino circuits can be analysed and compared with 65nm technology is used. The proposed work is based on 256 bit Manchester Carry chain(MCC) adders compared with different CMOS technologies.

KEYWORDS: Addition, Carry-Look ahead Adder (CLA), High Performance, propagation delay, CMOS technology, HSPICE tool

I.INTRODUCTION

In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic units, but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operation. The digital logic gates and circuits designed using dynamic domino technique is considerably faster than the logic gates and circuits designed with standard static logic style. Now four major performance parameters i.e. Power, area, delay and speed are focused by VLSI designer. A carry look ahead adder is a type of adder used in digital logic. It improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits.

In this paper Carry look ahead adder is designed and analyzed using standard CMOS technique. The Manchester carry chain adder (MCC) is the most popular dynamic (domino) CLA, is proposed with an implementation in VLSI. The MCC have enabled the development of multi-output domino gates which have given area and speed improvement with respect to single output. The efficiency of the MCC is trying to transfer its structure to static logic. In a report has been made of dynamic CMOS 4-bit CLA adder in multi-output logic which reduces the number of transistors which considered to a conventional schema. However, the simulation results not shown any speed improvement but reduce the delay.

II.RELATED WORK

The Basic operation of this model has the concept of carry look-ahead adders with a 4-bit as a input with an output of sum is generated and carry bits is propagated.

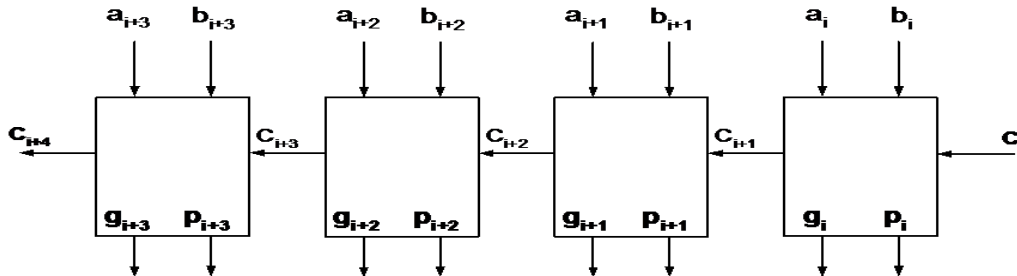


Figure:1 4bit adder as an example

Figure 1 shows the fast method of adding numbers is called carry-look ahead. This method does not require the carry signal to propagate stage by stage, causing a bottleneck. Instead it uses additional logic to expedite the propagation and generation of carry information[1].

The CLA solves the problem of delay it takes to propagate the carry, by calculating the carry signal in advance based on the input signal. The working of this adder can be understood by manipulating Boolean expressions dealing with full adder. The propagate 'Pi' and generate 'Gi' in a full adder is given by $P_i = x_{in} \oplus y_{in}$ Carry propagate $G_i = x_{in} \text{ and } y_{in}$ Carry generate

The new expressions for the output sum and the carryout are given by:

$$\text{sum} = S_i = P_i \oplus C_{i-1}$$

$$\text{carry_out} = C_{i+1} = G_i + P_i \text{ and } C_i$$

These equations show that a carry signal will be generated in two cases:

- 1) If both bits x_{in} and y_{in} are 1
- 2) If either x_{in} or y_{in} is 1 and the carry_{in} is 1.

Let's apply these equations for a 4-bit adder

$$C_1 = G_0 + P_0C_0$$

$$C_2 = G_1 + P_1C_1 = G_1 + P_1(G_0 + P_0C_0) = G_1 + P_1G_0 + P_1P_0C_0$$

$$C_3 = G_2 + P_2C_2 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0$$

$$C_4 = G_3 + P_3C_3 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0$$

Similarly we can write the general expression as

$$C_{i+1} = G_i + P_iG_{i-1} + P_iP_{i-1}G_{i-2} + \dots + P_iP_{i-1} \dots P_2P_1G_0 + P_iP_{i-1} \dots P_1P_0C_0.$$

The CLA algorithm was first introduced in several variants have been developed. The Manchester carry chain (MCC) is the most common dynamic (domino) CLA adder architecture with a regular, fast, and simple structure adequate for implementation in VLSI[5]. The recursive properties of the carries in MCC have enabled the development of multi-output domino gates, which have shown area-speed improvements with respect to single-output gates using 90nm technology.

In this brief, a new 8-bit carry chain adder block in multi-output domino CMOS logic is proposed. The even and odd carries of this adder are computed in parallel by two independent 4-bit carry chains[7]. Implementation of wider adders based on the use of the proposed 8-bit adder module shows significant operating speed improvement compared to their corresponding adders based on the standard 4-bit MCC adder module[8].

III. NEW HIGH SPEED ADDER IN DYNAMIC (DOMINO) CIRCUIT

The generate signal implemented in domino logic is shown in Figure 2. It consists of two inputs namely ai and bi and has one output gi. The two inputs are connected in series thus perform AND operation. The operation of the circuit is controlled by clock signal.

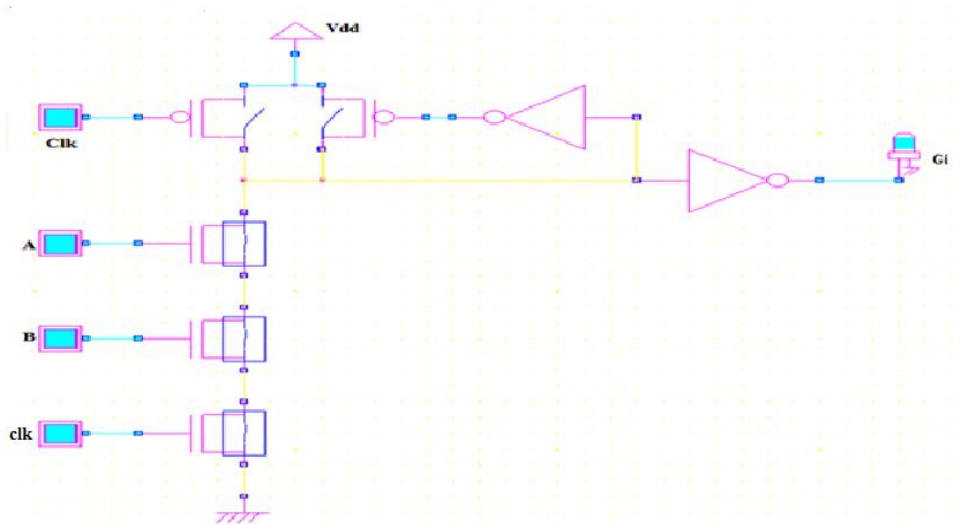


Figure: 2 Schematic Diagram of Generate Signal Implemented in Domino Logic

Figure 2 shows the implementation of generate signal in domino logic. The circuit will possess generally two state precharge state and evaluation state. If the clock signal goes to value '0', then the circuit will enter into precharge state and PMOS will get connected to ground and output will maintain the value of 0. If the clock makes the transition from 0 to 1 then the circuit will enter into evaluation state and the output depends on the input value. Since generate signal possess AND operation if both input are maintained at 1, 1 then the output gi will be maintained at 1 else the output value will be maintained at 0 i.e. $g_i = 0$.

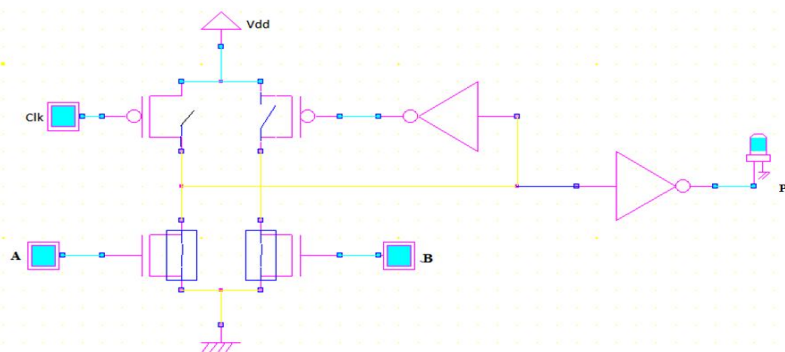


Figure: 3 Schematic Diagram of Propagate OR Signal

The propagate signal implemented in domino logic is shown in Figure 3. It consists of two inputs ai and bi and consists of one output signal pi. Here the propagate signal is implemented in OR operation. The propagate circuit is controlled by clock signal. If clk goes to '0', then the circuit will enter into precharge state and the output remains in 0 value. If clk value is 1, then the output value depends on input value. Since this propagate signal is OR operation based if any one of the inputs is 1, then output pi will maintain the value 1 else pi will have value 0.

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IV.SIMULATION RESULT AND DISCUSSION

In this section simulation results for carry look-ahead adder implemented in domino logic in 65nm technology. The following figures shows the simulation report with various parameter like power, voltage, temperature etc.,

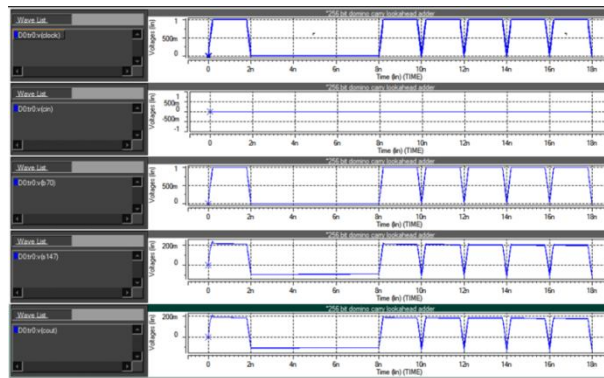


Fig. 4 Timing diagram of the 128-bit adder using domino logic

In the fig 4, it shows the result of 128 bits as an input. These input will provide the output as sum and carry. These outputs are obtained by varying a clock signal in the domino circuit 65nm technology.

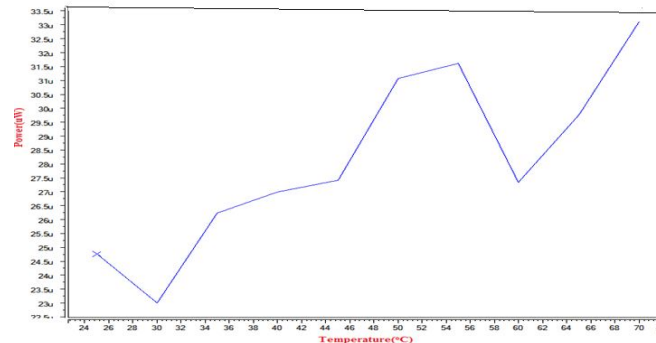


Fig.5 power vs temperature

Figure 5 shows the graph that compares the power with temperature. From the figure it illustrates that while the temperature increases, power of the circuit also get increases.

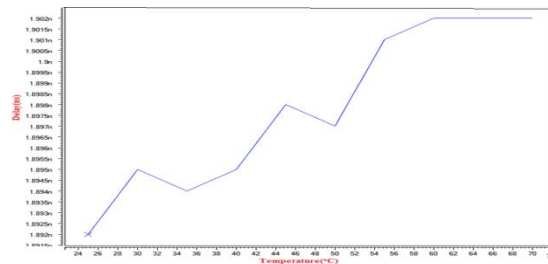


Fig. 6 total delay vs temperature

In fig 6, it shows the graph of total delay vs temperature. The temperature is focused on heat dissipation in the circuit so the performance of circuit reduces, delay has been increased accordingly.

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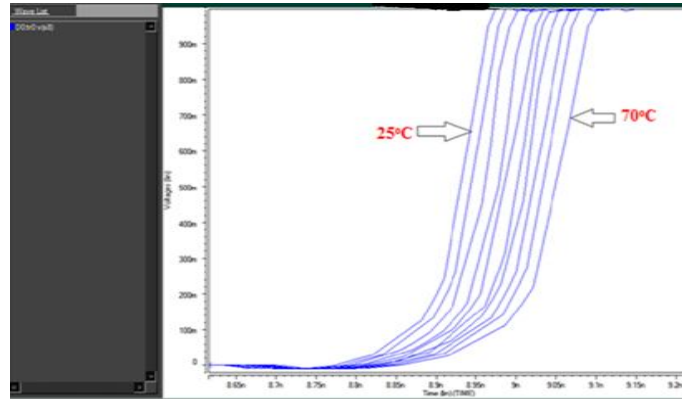


Fig.7 voltage vs temperature

In fig 7 it shows variation of voltage while the temperature has been varied from 25 °C to 70 °C.

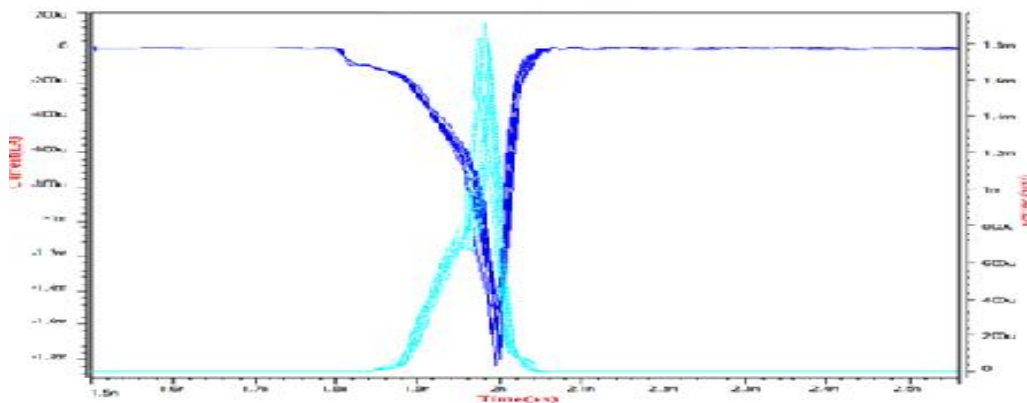


Fig.8 current vs time vs power

In fig.8 it shows the graph of current vs time vs power. When current is off condition the power also pursuing the same condition, it gets increased when current is in on.

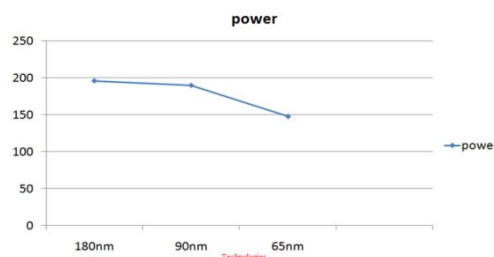


Fig.9 comparison with power and technology

In Fig.9 it shows the graph which compares the power and technologies (180nm,90nm,65nm).it depends on the supply voltage of the technology used ie (V_{DD}=1.0V).

V. CONCLUSION

In this paper the performance of 128-bit adder circuit designed using in dynamic (domino) circuit techniques is analysed in detail and its performance is compared with static adder circuits. The 128-bit adder circuit is simulated using L=65nm technology along with supply voltage V_{DD}=1.0V. The experimental results shows that these adder



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circuits gives superior performance compared to adder circuits designed using conventional domino techniques. Further, Manchester carry chain adder in 256-bit is used for increasing high speed and reduced delay in the domino circuit.

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BIOGRAPHY

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