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Gate Count Comparison of Different 16-Bit Carry Select Adders

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ABSTRACT: Addition is the most fundamental computational process encountered in digital system. An area efficient carry select adder is proposed in this paper by comparing the Gate count of Regular and Modified 16-bit carry select adders with a proposed Common Boolean Logic carry select adder. In this paper, Gate count evaluation of Regular, Modified and proposed designs are given in terms of INVERTER, NAND and NOR Gates. The comparison results shows that the common Boolean logic carry select adder structure require lesser number of gates than that of Regular and Modified 16-bit carry select adder.

KEYWORDS: Common Boolean Logic, Gate Count, Comparison

I. INTRODUCTION

Digital computers perform variety of information tasks. Among the functions encountered are the various arithmetic operations. The basic arithmetic operation is addition and is performed by different binary adders. The common and very useful combinational logic circuit which can be constructed using few basic logic gates. Any binary adder is made up from Inverter, AND, OR and XOR gates. In this paper the architectures of Regular, Modified and proposed carry select adders gate counts are given in terms of Inverter, Nand and Nor Gates.

The number of gates required for AND and OR gates in terms of Inverter, Nand and Nor are 1 1 0 and 1 0 1 respectively. Similarly the gate count required for XOR is given as follows. The Boolean expression for XOR is A'B+AB' and the circuit is given as shown in fig 1.

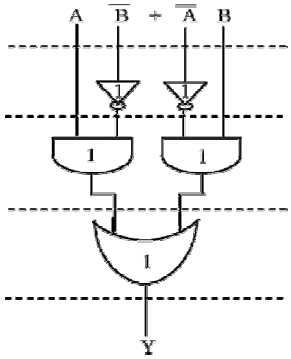

Fig.1 Xor gate

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In fig 1, there are 2 AND gates,1 OR gate,2 Inverters present. The total gate count in terms of Inverter, Nand, Nor gates are 5 2 1. Similarly the gate counts of different gates that are used in the Regular, Modified and Common Boolean Logic carry select adders architectures are given in the Table 1.

Table .1 Gate counts of Basic gates

Name / Gate Type	INVERTER	NAND	NOR
AND	1	1	0
OR	1	0	1
XOR	5	2	1
2x1 Mux	4	2	1
HALF ADDER	6	3	1
FULL ADDER	8	4	2

II. REGULAR 16-BIT CARRY SELECT ADDER

The Architecture of Regular 16-bit carry select adder is shown in fig 2. It has five groups, each is of different size.

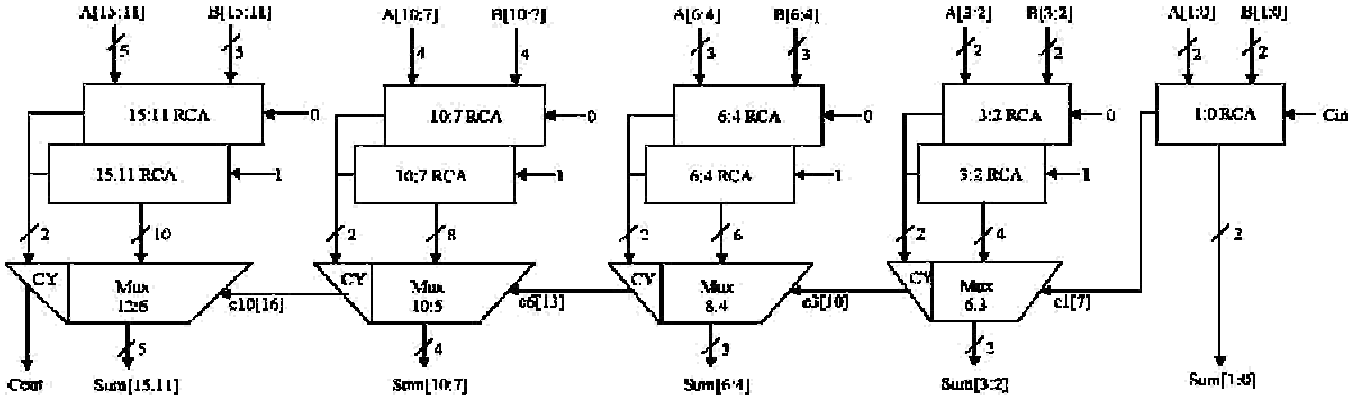

Fig. 2 Regular 16-bit Carry Select Adder

The Gate count evaluation of group (1) and group (2) is shown in fig 3.The group (1) has two full adders. The structure of it is shown in fig 3a. The Gate count in terms of Inverter, Nand and Nor gates is determined as follows.

Gate count= 2*Full Adders (FA)

= 2*14

= 28.

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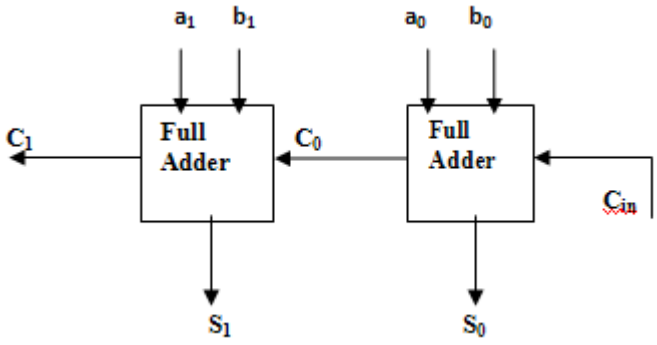

Fig. 3a Group (1)

Similarly, the structure of group (2) is shown in fig 3b. and the Gate count is determined as follows.
Gate count= 3 (FA) +1 (HA) +3 (2x1 Mux)
= 3*14+1*10+3*7
= 42+10+21

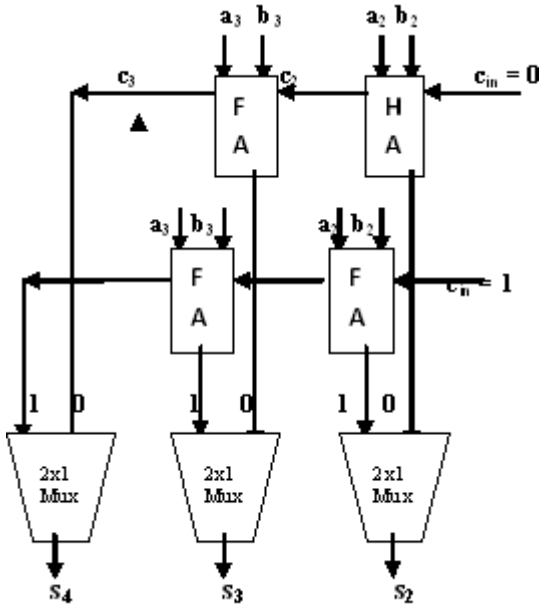

Fig. 3b Group (2)

In the same way the gate counts of remaining three groups are calculated. The gate counts of all five groups of Regular 16-bit carry select adder in terms of Inverter, Nand and Nor gates are given in Table 2. The total number of gates required for the above architecture is **530.**

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Table. 2 Gate counts of five groups of Regular carry select adder

Group Number	Total Gate Count
Group (1)	28
Group (2)	73
Group (3)	108
Group (4)	143
Group (5)	178

III. MODIFIED 16-BIT CARRY SELECT ADDER

The architecture of Modified 16-bit carry select adder is shown in fig 4. The difference between the regular and modified 16-bit carry select adders lies at c_{in}=1, that is, in regular carry select adder ripple carry adder is used where as in modified 16-bit carry select adder Binary to excess one converter is used for c_{in}=1. In Modified carry select adder also there are five different groups. The Gate count evaluation is shown in fig 5.

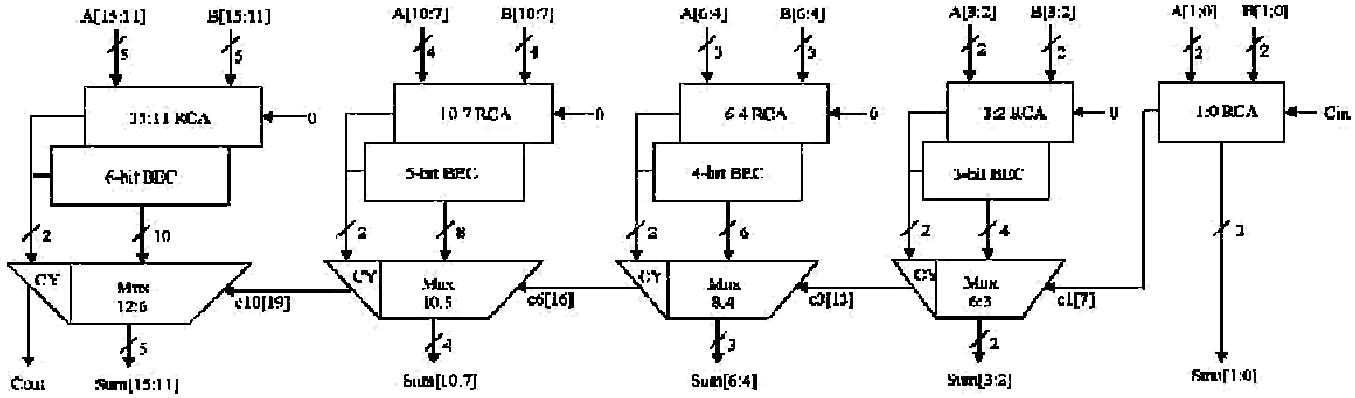

Fig. 4 Modified 16-bit Carry Select Adder

The Gate count evaluation of group (1) and Group (2) of fig 5 are determined as follows.

The Gate count =2*Full Adders (FA)

= 2*14

= 28.

The Gate count = 1FA+1HA+2XOR+1AND+1INVERTER+3MUX

= 1*14+1*10+2*8+1*2+1+3*7

= 64

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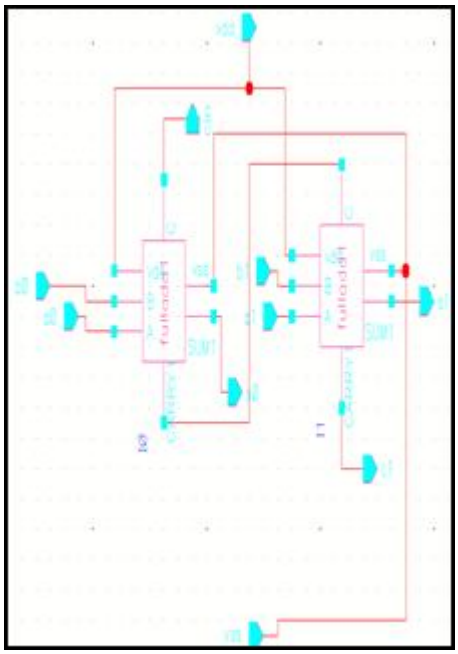

Fig. 5a Group (1)

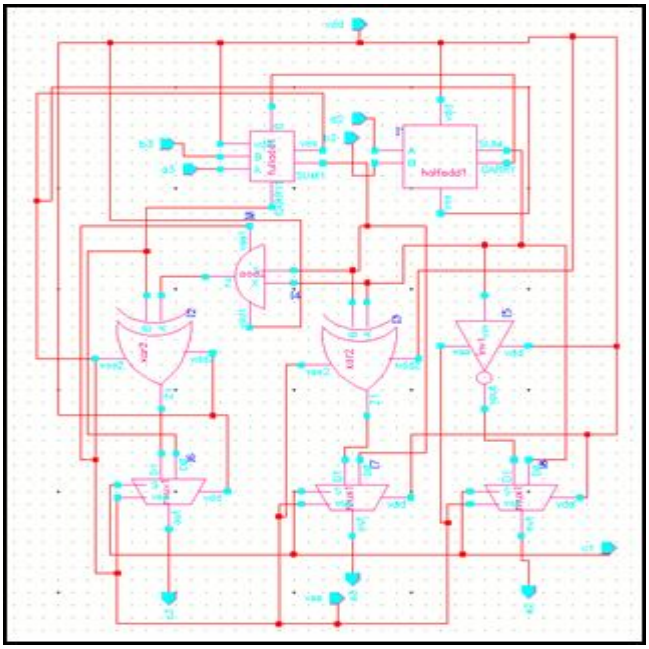

Fig. 5b Group (2)

Similarly, the remaining three Groups Gate counts are determined .The Gate counts of all five groups in terms of Inverter, Nand and Nor gates are given in Table 3.

Table 3. Gate Counts of five groups of Modified carry select adder

Group Number	Gate Count
Group (1)	28
Group (2)	64
Group (3)	95
Group (4)	126
Group (5)	157

The total number of gates for Modified 16-bit Carry select adder is **470.** By comparing the gate counts of above two architectures, the number of gates of the later architecture is reduced by 60.

IV. PROPOSED CARRY SELECT ADDER USING COMMON BOOLEAN LOGIC

The proposed carry select adder is constructed by using the common Boolean logic. This logic is given with full adder shown in the fig 6.

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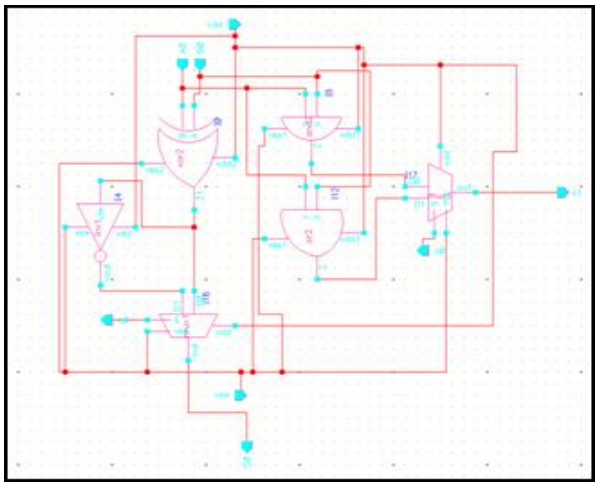

Fig. 6 One bit carry select adder using common Boolean logic

In this proposed architecture, XOR and AND gates are used instead of Full adders for c_{in}=0 and inverter from XOR and OR gates are used instead of full adders and Binary to Excess-1 converter for c_{in}=1. With the use of these gates, the gate count of this architecture is reduced. The gate count of proposed one bit carry select adder is given as follows.

The Gate count = 1XOR+1OR+1AND+1INVERTER+2MUX

= 1*8+1*2+1*2+1+2*7

= 27.

The truth table of full adder is given in Table 4.

Cin	A	B	S0	C0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table .4 Truth table of single bit carry select adder using common Boolean logic

Similarly, the gate count of 16-bit common Boolean logic using carry select adder is 16*27=**432**.The 16-bit proposed carry select adder is constructed from 'sixteen' similar one bit common Boolean logic.

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V. COMPARISON RESULTS

A comparison of different 16-bit carry select adders in terms of inverter, nand & nor gates are given where the 16-bit regular and modified carry select adders have different groups for c_{in}=0 and c_{in}=1 and the proposed common Boolean logic carry select adder has sixteen similar groups. Fig 7 shows the comparison of gate counts of five different groups of regular and modified carry select adders.

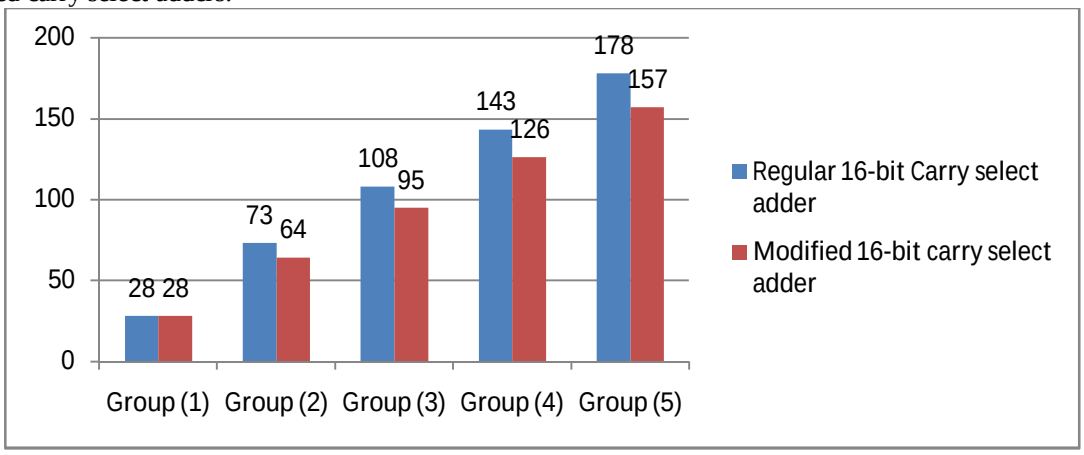

Fig. 7 Gate count comparison

Fig 8 shows comparison of total number of gates required for 16-bit regular, modified and proposed carry select adders. Comparing 16-bit regular and modified with proposed carry select adders the number of gates for the proposed carry select adder reduced by 98 and 38 respectively.

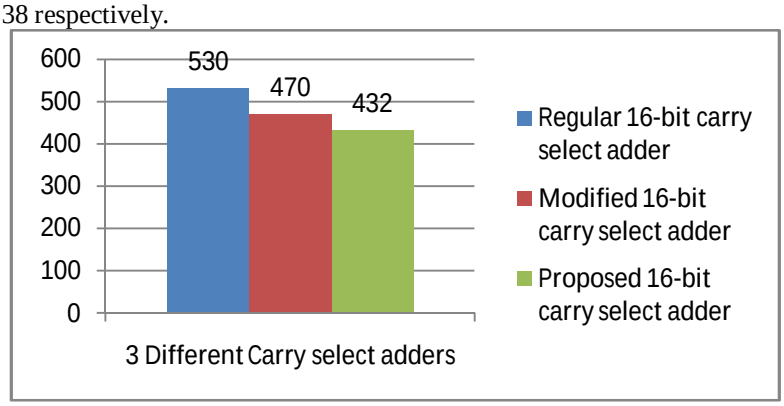

Fig. 8 Gate counts of carry select adders

VI. CONCLUSION

In this paper, comparison of different 16-bit carry select adders are given and is determined that proposed carry select adder has reduced gate count than the other two. The percentage decrease in gate count of proposed 16-bit common Boolean logic carry select adder when compared with 16-bit regular and modified carry select adders are 18.5% and 8% respectively.

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BIOGRAPHY

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