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FPGA IMPLEMENTATION OF DSWG USING CORDIC ALGORITHM

K.Prasanna Kumar[1], K.V.Ramana Rao[2], R.Vijaya Durga[3]

(M.Tech), Dept. of ECE, Pydah College of Engg. And Tech., Visakhapatnam, India.

(M.Tech)., Associate Professor, Dept. of ECE, Pydah College of Engg. And Tech., Visakhapatnam, India.

(M.Tech), Dept. of ECE, Pydah College of Engg. And Tech., Visakhapatnam, India.

ABSTRACT: The Coordinate Rotational Digital Computer (CORDIC) algorithm is another classic approach for sine wave generation. This trigonometric iteration based approach relies on vector rotations for performing successive mapping between polar and rectangular co-ordinates (and vice versa)

Keywords: Coordinate Rotation Digital Computer (CORDIC), Cosine/Sine, FPGA, Recursive Architecture

I. INTRODUCTION

The CORDIC relies on predetermined phase, amplitude and frequency values for calculating points on Sine wave. The CORDIC has several important areas of application like generation of Sine and Cosine functions, Calculation of discrete sinusoidal transforms like Fast Fourier Transform(FFT), Discrete sine/cosine transforms(DST/DCT), house holder transform(HT) etc.[5-7].Many variations have been suggested for efficient implementation of CORDIC with less number of iterations over the conventional CORDIC algorithm[8-10].In efficient scale-factor compensation techniques are proposed, which adversely affect the latency/throughput of computation..The CORDIC's advantage over more traditional LUT based approaches lies on its capacity of producing simultaneous in-phase and quadrature components, as well as being a bit-recursive algorithm. The particular architecture hereby presented generates the phase of the sine by self on enable and performs the CORDIC vector rotation in order to produce sine wave values at the rate of 4096 samples per cycle. The implementation of DSWG (Digital sinusoidal wave generation) was partitioned into two main blocks: a Sine magnitude generator (SMG) block and a CORDIC logic processor (CLP) block. The SMG produces the phase increments which drives the CLP, while performing replication in order to obtain the complete cycle of sine wave. Meanwhile, the CLP block performs the vector rotation and generates the sine magnitude.This rest of the paper is structured as follows. Section II reviews the existing CORDIC algorithms. The proposed CORDIC architecture is discussed in section IV. Section V details the field-programmable gate array (FPGA) implementation and comparison with the existing architectures, and section VI concludes this paper.

II. BRIEF OVERVIEW OF CORDIC ALGORITHM

The CORDIC algorithm [3], can be derived from the general rotation transform, as stated on the equations below:

$x' = x \cos \Phi - y \sin \Phi$ (1)

$y' = y \cos \Phi + x \sin \Phi$ (2)

$$\begin{bmatrix} x_{i+1} \\ y_{i+1} \end{bmatrix} = K_i \begin{bmatrix} 1 & -\mu_i . \tan\alpha_i \\ -\mu_i . \tan\alpha_i & 1 \end{bmatrix} . \begin{bmatrix} x_i \\ y_i \end{bmatrix} \quad (3)$$

Equations 1 and 2 express the transformed Cartesian coordinates after a vector rotation by an angle of Φ degrees. The before mentioned equations can be written as follows:

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$x' = \cos \Phi .[x - y \tan \Phi]$ (4)

$y' = \cos \Phi .[y + x \tan \Phi]$ (5)

Restricting the rotation angle so that $\tan \Phi = \pm 2^{-i}$, the multiplication by tan Φ can be reduced to a simple shift operation, meanwhile arbitrary angles can be expressed in terms of these known restricted angles. So a vector rotation by an arbitrary angle can be achieved by successive elementary rotations by known angles.

In equations (4) and (5), cos Φ is constant, allowing these equations to be written as follows:

$$x_{i+1} = K_i[x_i - y_i . d_i . 2^{-i}] \quad (6)$$

$$y_{i+1} = K_i[y_i + x_i . d_i . 2^{-i}] \quad (7)$$

$$\emptyset_{i+1} = \emptyset_i - d_i . tan^{-1}(2^{-i}) \quad (8)$$

Where

$$K_i = \cos(tan^{-1}2^{-i}) = \frac{1}{\sqrt{1+2^{-2i}}} \quad (9)$$

$d = \text{sign}(\Phi)$ (10)

As the number of iterations increases so does the accuracy of the resulting Cartesian coordinate values. By feeding angles from 0^o to 360^o for vector rotation, the resulting x and y coordinates represent the corresponding sine and cosine scaled magnitudes. This can be achieved through pipelining the rotations. Pseudo code for the pipeline process is as follows:

Initiation: Given x, y and Ø

For n=0: N-1

Calculate K

Calculate d_n^n

Calculate $x_{i+1}, y_{i+1}, \emptyset_{i+1}$

End loop

At the N-1 iteration of the loop, the values of x_N and y_N are obtained. Permitting the calculation of X_{out} and Y_{out} as seen in the equations below(For the given rotation angle, X_{out} represents the sine magnitude and Y_{out} represents the cosine magnitude):

$$X_{out} = {}^{x_N}/_{K_N} \quad (11)$$

$$Y_{out} = {}^{y_N}/_{K_N} \quad (12)$$

Where

$$K_N = \prod_0^{N-1} 1 \Big/ (\sqrt{1 + 2^{-2i}}) \quad (13)$$

A. CORDIC ALGORITHM IMPLEMENTATION

1. PHASE ANGLE MAPPING:

Phase angle and sine magnitude are represented in this implementation with 16 bits, scaled value of 360^o is 2^{16}.

$1^o = 2^{16}/(360^o) = 182$ (14)

Since the choice of sampling rate $f_s = 4096$ per cycle

$1^o = 4096/360 = 11.3778$ samples (15)

Therefore, the sampling duration should be

$182/11.3778 = 16$(approx)and resolution $= 1^o/11.3778 = 0.0879^o$(approx) (16)

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2. MAGNITUDE SCALING:

Magnitude is represented with 16 bits, out of these MSB is used to represent sign and the rest 15 bits are used to represent the magnitude. Output represents the values in the 0 to +1 range. The results can be derived as follows:
Sin0 = 0 is represented by the minimum values possible with 15 bits.
Sin90 = 1.0 is represented by the maximum values possible with 15 bits, i.e., 2^{15}.
Therefore output scaling factor = $1/2^{15}$

III. GENERALIZED MICRO-ROTATION

In the proposed generalized micro-rotation sequence, we perform multiple iterations of basic-shift, followed by non-repetitive unidirectional iterations of the micro-rotations corresponding to other shift indices, to minimize the number of iterations and achieve adequate range of convergence.
Organization of micro-rotation sequence:
In the proposed scheme we represent the rotation angle "θ" as

$$\theta = n_1 . \alpha_s + \sum_{i=1}^{n_2} \alpha_{s_i} . n = n_1 + n_2 \quad (17)$$

Where α is the elementary angle corresponding to the basic-shift, are elementary angles for other shifts, n_1 and n_2 are non-negative integers and n represents the total number of iterations. If we do not use any micro-rotation of angle α_s then n_1 = 0 and$n_2 = n$. On the other hand, if the desired angle of rotation "θ" is a multiple of then n_2 = 0 and$n_1 = n$.

A. DEFINING THE ELEMENTARY ANGLES

The elementary angles α_s and α_{s_i} are given by $\alpha_s = 2^{-s} and\ \alpha_{s_i}=2_i^{-s}$ (18)
Where s is the basic-shift and $s_i > s$ is the shift for i^{th} iterations. For basic-shift = 2, we can find $\alpha_s = 7\pi/88$ and for basic-shift=3, we can find$\alpha_s = 7\pi/176$.

B. GENERALIZED MICRO-ROTATION SEQUENCE IDENTIFICATION

We identify the micro-rotations depending on the bit representation of the desired rotation angle in radix-2 system using most-significant-1 detector. For this we restrict the maximum rotation angle to $\frac{\pi}{4}$ $radians$ as the coordinate space [0,2π] can be mapped to [0,$\frac{\pi}{4}$] using octant symmetry of sine and cosine functions. If the most significant-1 location(M) of the rotation angle "θ" is smaller than the basic-shift "s" elementary angle of basic-shift would be used for the CORDIC iteration for a fixed word-length of n-bit, the shift (s_i) for elementary angle is given by
s_i= N-M. (19)

Table 1:
Input: angle tobe rotated (θ_i)
Begin
M= Most Significant-1 Location of θ_i
If (M==15) then
α = 0.25 radians
Shift s_i= 2 and $\theta_{i-1} = \theta_i - \alpha$
Else
Shift $s_i = 16 - M$

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$\theta_{i-1} = \theta_i$ With $\theta_i[M] = '0'$
End

IV. DESIGN ARCHITECTURE

This design enables with EN signal and triggers with positive edge triggered clock and resets with RST signal is designed to generate the sine wave samples. Frequency of the oscillations depends on the clock frequency. It is designed to produce one sample for every 0.0879^o (approx).

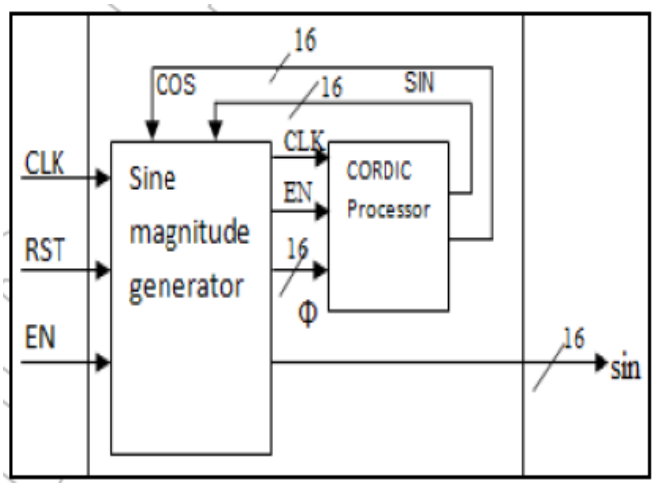

Fig-1: FPGA Design Architecture of sine wave generator

Sequential logic-1 shown in fig1 generates the next state variables and D-flip flops: DA and DB derive present state variables from the next state variables. These present state variables are used as select lines for MUX M1, which outputs the initial phase angle for the given coordinate. Combinational circuit-1 derives the select lines for MUX:-M2 to choose either initial phase value or running phase value to get add or subtracted by phase step value held resolution register. Add-sub unit performs either addition or subtraction on proceeding
phase value and phase step value held by resolution register. D-flip-flops – D0 to D15 holds the add-sub unit result for a clock cycle.

A. SIGN MAGNITUDE GENERATOR

This module feeds the phase to CORDIC module on enable and replicates the positive and negative quarter waves to obtain the complete cycle. Sign Magnitude growth through the full cycle is described in fig2.

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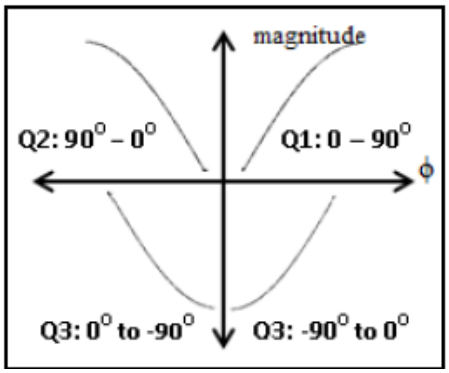

Fig-2: Angle mapping over the full cycle of sine wave

B. CORDIC PROCESSOR

CORDIC processor consists of CORDIC pipe and CORDIC rotation module. Pipe line processor executes the iterations specified in the pseudo code and CORDIC rotation module performs the vector rotation by the angle specified by the pipeline processor.

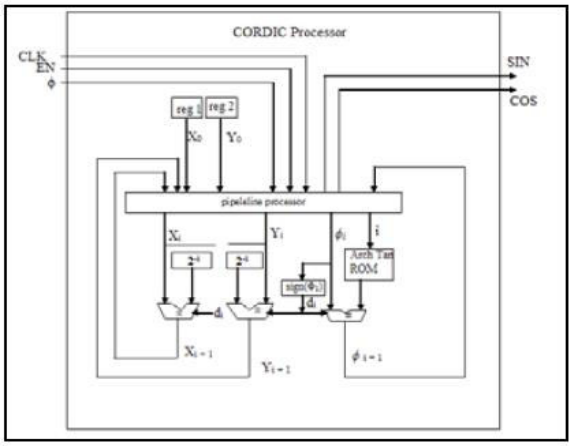

Fig-3: CORDIC Processor

CORDIC processor performs the competitions described in equations 6, 7, 8. In this circuit register 1 holds the value 19898. It is a scaled (2^{16}) value of 0.6072(K_N) and reg2 holds 16 Zero-bits. Arch tan table is basically ROM which stores arch tan table described in CORDIC algorithm.

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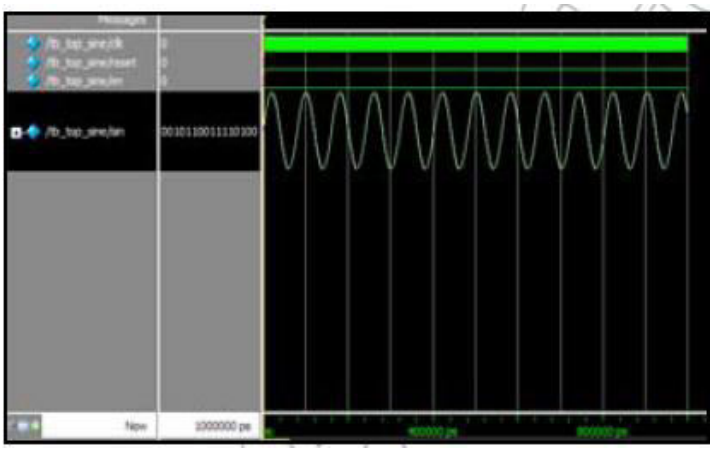
SIMULATION RESULT



Synthesis Report:

IO Ports

PORT	WIDTH	DIRECTION	DESCRIPTION
CLK	1	Input	System Clock
EN	1	Input	Clock Enable Signal
RESET	1	Input	Resets the Core
Sin	16	Output	Sine Output

Table2: List of IO Ports for Sine/Cosine CORDIC Core

V. FPGA IMPLEMENTATION

The proposed architecture is coded in Verilog and synthesized using Xilinx ISE12.1I to be implemented in Xilinx Spartan 3E (XC3S200TQ144) device.

VI. CONCLUSIONS

To increase throughput, pipelined CORDIC processors is used in this paper with the penalty that the pipelined structure would require large amount of chip area [1]. The CORDIC algorithm is suitable for the DDS with more than 14 output bits, where the sign Look-up table even with a compression is still too large for high speed operation. Cosine points also can be generated along with sign points because CORDIC algorithm can calculate both in-phase and quadrature components simultaneously [3]. Through programming the constant value (equ 13) in reg1 shown in fig3, amplitude of the sign wave can be tuned. With this implementation sine wave can be generated with the error of 0.0021% at peaks and zero crossings. This signed precision is obtained after skipping without generation the 77 samples at these crossings.

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