ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 7, July 2014

Five-Input Complex Gate with an Inverter Using QCA

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ABSTRACT:This paper presents the basics of quantum dot cellular automata along with the QCA logic devices such as the QCA wire, inverter and the majority gate. The four phases of the clocking have been discussed and also the implementations of the complex gate have been done using the QCADesigner tool. The logical structures such as NAND and NOR gates using a quantum dot cellular automata complex gate composed of 3 input majority gate and an inverter have been implemented.

KEYWORDS: QCA, majority gate, inverter, complex gates, QCA Designer.

I.INTRODUCTION

Current silicon transistor technology faces challenging problems, such as high power consumption and difficulties in feature size reduction. Nanotechnology is an alternative to these problems. The Quantum dot cellular automata (QCA) is one of the attractive alternatives [1]. Since QCAs were introduced in 1993 by lent et al, and experimentally verified in 1997. QCA is expected to achieve high device density, extremely low power consumption and very high switching speed.QCA structures are constructed as an array of quantum cells with in which every cell has an electrostatic interaction with its neighboring cells [2]. QCA applies a new form of computation, where polarization rather than the traditional current, contains the digital information. In this trend, instead of interconnecting wires, the cells transfer the information throughout the circuit [4].
This paper describes the design of different logical structures in QCA such as NAND and NOR. These structures are designed based on the basic logical devices. The paper is organized as follows, the background of QCA technology is explained in section 2. Section 3, provides the QCA clocking and section 4 describes the QCA Designer tool. Section 5 shows the design and implementation of logical structures in QCA using three input majority and an inverter. Simulation results follow in section 6 and conclusions are presented in section 7.

II.BACKGROUND

A. QCA basics

QCA technology is based on the interaction of bi-stable QCA cells constructed from four quantum dots. The cell is charged with two free electrons, which are able to tunnel between adjacent dots. These electrons tend to occupy antipodal sites as a result of their mutual electrostatic repulsion. Thus, there exist two equivalent energetically minimal arrangements of the two electrons in the QCA cell, as shown in Fig. 1. These two arrangements are denoted as cell polarization P= +1and P= -1.By using cell polarization P =+1 to represent logic “1” and P =-1 to represent logic “0,” binary information is encoded in the charge configuration of the QCA cell [2][5].

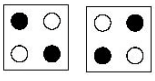

Fig.1.QCAcellpolarization

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B. QCA logic devices

The fundamental QCA logic primitives include a QCA wire, QCA inverter, and QCA majority gate[4]-[6], as described below.

QCA Wire: In a QCA wire, the binary signal propagates from input to output because of the electrostatic interactions between cells. The propagation in a 90˚ QCA wire is shown in Fig. 2. Other than the 90˚ QCA wire, a 45˚ QCA wire can also be used. In this case, the propagation of the binary signal alternates between the two polarizations [4].

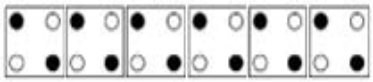

Fig. 2.1. QCA wire (90^0)

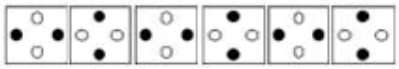

Fig. 2.2 QCA wire (45^0)

QCA inverter: The QCA cells can be used to form the primitive logic gates. The simplest structure is the inverter shown. Fig. 3, which is usually formed by placing the cells with only their corners touching. The electrostatic interaction is inverted, because the quantum-dots corresponding to different polarizations are misaligned between the cells [3].

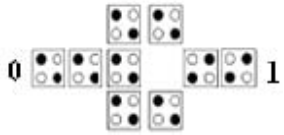

Fig. 3.QCA inverter

*QCAMajorityGate:*TheQCAmajoritygateperformsathree-inputlogicfunction.AlayoutofaQCAmajoritygateisshowninFig.4.1.Assumingtheinputsarea,bandc,thelogicfunctionofthemajoritygateis

$$M(a,b,c)=ab+bc+ac. \quad (1)$$

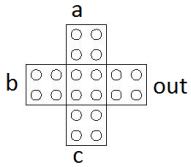

Fig.4.1.QCAmajoritygate

Thetendencyofthemajoritydevicecelltomovetoagroundstateensuresthatittakesonthepolarizationofthemajorityofitsneighbours.Thedevicecellwilltendtofollowthemajoritypolarizationbecauseitrepresentsthelowestenergystate[3].Byfixingthepolarizationofoneinputtotheqcamajoritygateaslogic “1” orlogic “0” anANDgateorORgatewillbeobtained,respectively,asshowninFig.4.2.

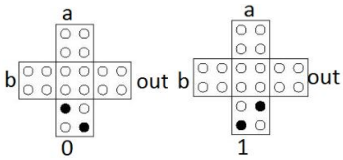

Fig.4.2.2-inputANDand2-inputORgates

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ISSN (Online): 2278 – 8875

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III.CLOCKING

TheQCAcircuitsrequireaclock,notonlytosynchronizeandcontrolinformationflowbutalsotoprovidethepowertorunthecircuitsincethereisnoexternalsourceforpoweringcells.Withtheuseoffourphasesclockingschemeincontrollingcells,QCAprocessesandforwardsinformationwithincellsinanarrangedtimingscheme.Cellscanbegroupedintozonessothatthefieldinfluencingallthecellsinthezoneswillbethesame.Azonecyclesthrough4phases.Inthe**Switch**phase,thetunnelingbarriersinazoneareraised.Whilethisoccurs,theelectronswithinthecellcanbeinfluencedbytheColumbiccharges ofneighboringzones.Zonesinthe**Hold**phasehaveahightunnelingbarrierandwillnotchangestate,butinfluenceotheradjacent.Lastly,the**Release**and**Relax**decreasethetunnelingbarriersothatthezonewillnotinfluenceotherzones.Thesezonescanbeofirregularshape,buttheirsizemustbewithincertainlimitsimposedbyfabricationanddissipationconcerns.Properplacementofthesezonesiscriticaltodesignefficiency.Thisclockingmethodmakesthedesignof QCAdifferentfromCMOScircuits.[7].

TheFig.5.Showsthefouravailableclocksignals.Eachsignalisphaseshiftedby90˚degrees.Whentheclocksignalislowthecellsarelatched.Whentheclocksignalishighthecellsarerelaxedandhavenopolarization.Inbetweenthecellsareeitherlatchingorrelaxingwhentheclockisdecreasing/increasingrespectively.

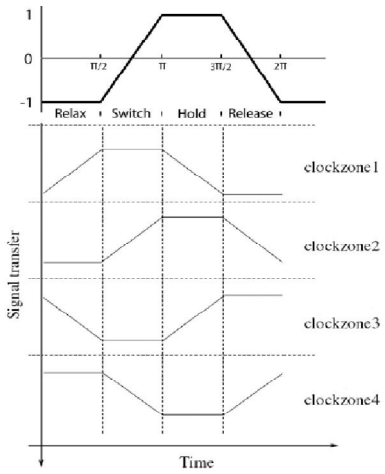

Fig. 5.Four phases of the clock.

IV.QCA DESIGNER TOOL

QCA logic and circuit designers require a rapid and accurate simulation and design layout tool to determine the functionality of QCA circuits. QCADesigner gives the designer the ability to quickly layout a QCA design by providing an extensive set of CAD tools. As well, several simulation engines facilitate rapid and accurate simulation. It is the first publicly available design and simulation tool for QCA. Developed at the ATIPS Laboratory, at the University of Calgary, QCADesigner currently supports three different simulation engines, and many of the CAD features required for complex circuit design. [8],[9].

V. QCA IMPLEMENTATION

The AND and OR gates are realized by fixing the polarization to one of the inputs of the majority gate to either P=-1(logic 0) or P=1(logic 1).
The same logic is used in the five-input complex gate with an inverter. This gate is composed of a 3-input majority gate which is placed in the middle of the complex gate. Here the input ‘e’ functions as a control input that is used to specify the functionality of the circuit. The remaining four inputs a, b, c and d are used to implement logical functions such as AND and OR. This implementation along with an inverter gives the logical functions NAND and NOR. The two cell-inverter is created by translating the output cell ‘Y’ by 9 nm horizontally. The functionality of this gate for four input

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NAND and NOR configurations has been simulated using QCA Designer. Fig. 6 shows five-input complex gate with a majority gate placed in the middle and a two cell-inverter made by translating the output Y.

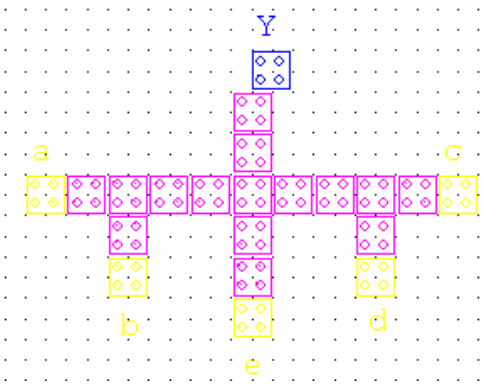

Fig.6 Five-Input complex gate with an inverter

A. *Four-Input NAND Gate*

The five-input gate of Fig. 6 can be used to form a 4-input NAND gate as shown in Fig. 7.1 by restricting input e to have a fixed polarity that is equal to -1. The selection of e is unique, either a or b can be restricted rather than e, and similarly c or d can be selected for restriction rather than g. For the example circuit as shown in Fig. 8, the function represented is $Y=\overline{abcd}$

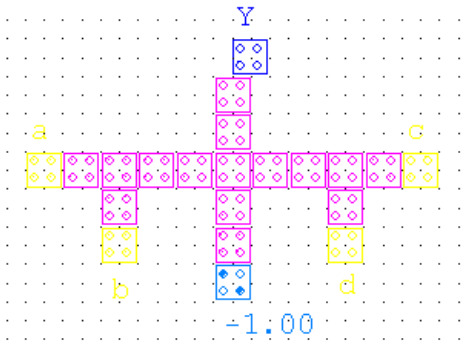

Fig.7.1 Four input NAND gate

B. *Four-Input NOR Gate*

Similarly, the five-input gate of Fig. 6 can also be used to form a 4-input NOR gate as shown in Fig. 7.2. For this configuration the input e is restricted to have a fixed polarity that is equal to 1. As for the NAND gate, the selection of e is unique The function represented is $Y=\overline{a+b+c+d}$

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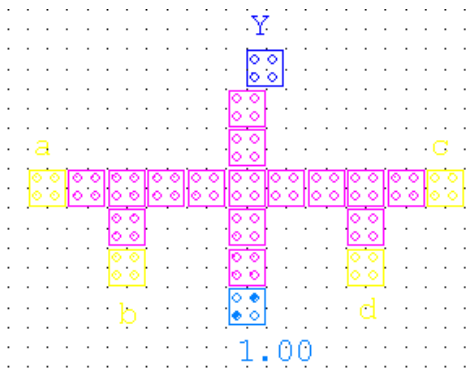

Fig. 7.2 Four input NOR gate

VI.SIMULATION RESULTS

With QCADesigner, the circuit functionality is verified. The following parameters are used for a bistable approximation: Cell size 18nm, Number of samples 12800, Convergence tolerance 0.001000, Radius of effect 65nm, Relative permittivity 12.9, Clock high 9.8e-22J, Clock low3.8e-23J, Clock amplitude factor2, Layer separation 11.5nm, Maximum Iterations per sample 100.

Fig.8.1 Simulation result for four input NAND gate

Fig.8.2 Simulation result for four input NOR gate

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VII.CONCLUSION

The logical structures such as NAND and NOR using five-input complex gate composed of a 3-input majority gate and a two cell inverter have been designed. One of these inputs typically function as control inputs to determine the logical structure formed by the four other inputs to the circuit. This five-input gate can be configured as a four-input NAND gate and a four-input NOR gate which are verified through simulation results.

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