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# DESIGN OF INTERPOLATION FILTER FOR WIDEBAND COMMUNICATION SYSTEM

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**Abstract:** Interpolation filters are integral part of a modern communication transmitter. This paper presents the design and FPGA implementation for a digital up converter or interpolation filter for a WiMAX Communication system. Multistage implementation approach has been used to reduce the hardware requirement. The results have been presented for a xc3sd1800a-4fg676 FPGA device.

**Keywords:** Digital Up Converter, FPGA, Interpolation, Multistage, WiMAX.

## I. INTRODUCTION

Modern signal processing problems are often solved in the digital domain due to the availability of powerful VLSI circuits which allow to perform complex operations in real-time, without the well-known shortcomings of analog implementations. The source signal is transformed into the digital domain by an A/D converter. All data processing, e.g. filtering, shaping, mixing etc., is done in the digital domain and only the final result is converted back to analog. To overcome the degradation caused by successive A/D-D/A conversion, all processing blocks must have digital interfaces. Depending on the available bandwidth of the channel, the required quality, and the data rate of the interfaces a wide variety of sample rates are used. The incorporation of all these systems is however trouble-free, if a sample-rate converter is used at each interface. Sample-rate conversion is used in the field of communications systems, speech processing systems, antenna systems and radar systems etc.

Many types of sampling have been discussed in the literature including non-uniform sampling, uniform sampling, and multiple function uniform sampling. The most common form of sampling is periodic sampling in which

$$q(t) = t/T = n \qquad (1)$$

i.e., the samples $x_D(n)$ are uniformly spaced in the dimension $t$, occurring $nT$ apart. For uniform sampling we define the sampling period as $T$ and the sampling rate as

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$$F = \frac{1}{T} \tag{2}$$

It is necessary that the sampling rate $F$ be chosen to satisfy the requirements of the Nyquist sampling theorem. The sampling rate $F$ is a fundamental consideration in many signal processing techniques and applications. It often determines the convenience, efficiency, and accuracy in which the signal processing can be performed. The process of digitally converting the sampling rate of a signal from a given rate $F = \frac{1}{T}$ to a different rate $F' = \frac{1}{T'}$ is calledsampling rate conversion. When the new sampling rate is higher than the original sampling rate, the process is called interpolation, whereas the process of digitally converting the sampling rate of a signal from a given rateto a lower rate is called decimation.Fig.1 provides a general description of a sampling rate conversion system.

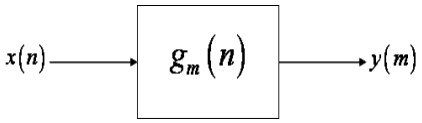


**Fig. 1 Basic process of digital sampling rate conversion.**

The ratio of sampling periods of $y(m)$ and $x(n)$ can be expressed as a rational fraction,

$$\frac{T'}{T} = \frac{F}{F'} = \frac{M}{L} \tag{3}$$

where $M$ and $L$ are integers.

Forlinear time-varying systems, each output sample $y(m)$) can be expressed as a linear combination of input samples $x(n)$. Mathematically $y(m)$ can be expressed as

$$y(m) = \sum_{n=-\infty}^{\infty} g_m(n)x([nm/L]-n) \tag{4}$$

In the trivial case when T' = T, or L = M = 1, equation (4) reduces to the simple time-invariant digital convolution equation

$$y(m) = \sum_{n=-\infty}^{\infty} g(n)x(m-n) \tag{5}$$

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## II. SAMPLING RATE UP CONVERSION

If the sampling rate is increased by an integer factor $L$, then the new sampling period $T'$ is

$$\frac{T'}{T} = \frac{1}{L} \tag{6}$$

and the new sampling rate $F' = LF$. This process of increasing the sampling rate of a signal $x(n)$ by $L$ implies that we must interpolate $L-1$ new sample values between each pair of sample values of $x(n)$.

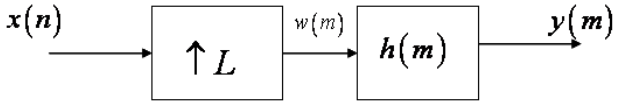


**Fig. 2Block diagram of Interpolator**

Fig. 2 shows the conceptual block diagram of interpolator. For interpolation by factor $L$, $L-1$ zero values have to be inserted between each pair of samples of $x(n)$, resulting in the signal, $w(m)$ given as

$$w(m) = \begin{cases} x(m/L), & m = 0, \pm L, \pm 2L, .... \\ 0, & otherwise \end{cases} \tag{7}$$

To recover the baseband signal of interest and eliminate the unwanted higher frequency components it isnecessary to filter the signal $w(m)$ with a digital low-pass filter, which approximates the ideal characteristic

$$\tilde{H}(e^{j\omega'}) = \begin{cases} G, & |\omega'| \le \frac{2\pi FT'}{2} = \pi / L \\ 0, & otherwise \end{cases} \tag{8}$$

If $H\left(e^{J\omega'}\right)$ denote the frequency response of an actual filter that approximates the characteristic in (8), then

$$Y(e^{j\omega'}) = H(e^{j\omega'})X(e^{j\omega' L}) \tag{9}$$

and from(8),using the approximated value of $H\left(e^{J\omega'}\right)$, (20) can be written as

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$$Y(e^{j\omega'}) = \begin{cases} GX(e^{j\omega' L}), & |\omega'| \le \pi / L \\ 0, & otherwise \end{cases} \qquad (10)$$

## III. DESIGN OF INTERPOLATION FILTER

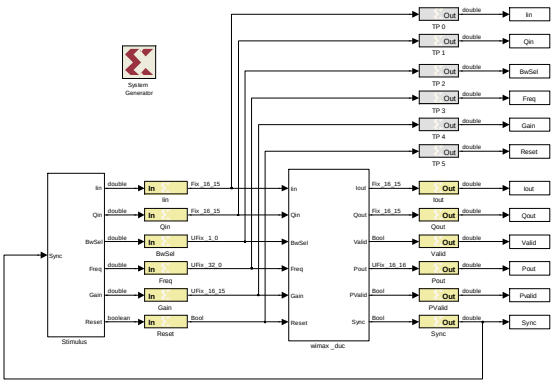


**Fig.3 System Generator Model for Interpolation Filter**

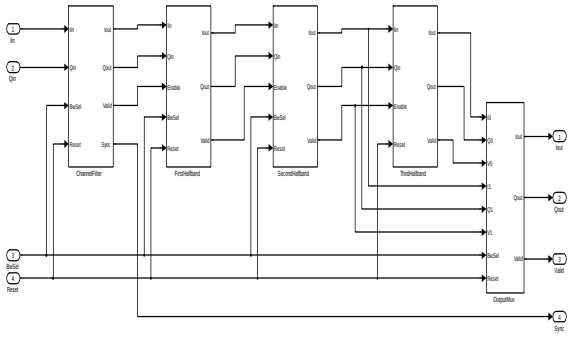


**Fig. 4 Internal View of Multistage Implementation**

Figure 3 show the complete setup developed using system generator and Figure 6 shows the details of DUC module. Figure 4 shows the internal view of multistage implementation of interpolation filterThe setup shown in Figure 3 has been simulated and synthesized using ISE 9.2i software. Table 1 shows the resources used by the design for xc3sd1800a-4fg676 FPGA device.

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**Table 1. Resource Utilization**

| Device Utilization Summary | | | | [-] |
|---|---|---|---|---|
| **Logic Utilization** | **Used** | **Available** | **Utilization** | **Note(s)** |
| Number of Slice Flip Flops | 1,968 | 33,280 | 5% | |
| Number of 4 input LUTs | 1,288 | 33,280 | 3% | |
| **Logic Distribution** | | | | |
| Number of occupied Slices | 1,733 | 16,640 | 10% | |
| Number of Slices containing only related logic | 1,733 | 1,733 | 100% | |
| Number of Slices containing unrelated logic | 0 | 1,733 | 0% | |
| **Total Number of 4 input LUTs** | 1,459 | 33,280 | 4% | |
| Number used as logic | 462 | | | |
| Number used as a route-thru | 171 | | | |
| Number used as Shift registers | 826 | | | |
| Number of bonded IOBs | 134 | 519 | 25% | |
| IOB Flip Flops | 48 | | | |
| Number of BUFGMUXs | 1 | 24 | 4% | |
| Number of DSP48As | 17 | 84 | 20% | |
| Number of RAMB16BWERs | 2 | 84 | 2% | |

From Table 1, it has been concluded that the proposed design uses only very small number of FPGA resources.

## IV. CONCLUSION

DUC is in integral part of a digital communication receiver and its multistage design leads to the requirement of less number of FPGA resources. This paper shows the successful implementation of DUC for a WiMAX system. The resources utilized by the proposed design are well below the hardware utilization reported in previous works.

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