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Design of 16-bit Heterogeneous Adder Architectures Using Different Homogeneous Adders

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ABSTRACT: Adders are digital circuits that perform addition operation. There are various types of adder structures such as Ripple carry adder (RCA), carry look ahead adder (CLA) , carry select adder (CSLA) , carry save adder(CSA), carry skip adder, carry increment adder and so on. Again CSLA is of two types that is linear carry select adder (LCSLA) & square root carry select adder (SQRT CSLA). To design an efficient adder circuit in terms of area, power and speed is one of the challenging task in modern VLSI design field. In this paper performance analysis of different adder structures like RCA, CLA, LCSLA and SQRT CSLA has been carried out and then a Heterogeneous adder structure is proposed, which compose of four different sub homogeneous adders (RCA, CLA, LCSLA and SQRT CSLA). The heterogeneous adder structure is used to demonstrate the tradeoffs between the speed and area. In this paper, all adder structures i.e., RCA, CLA, LCSLA and SQRT CSLA are to be designed and are to be compared with each other in terms of delay and area. Then by using the homogeneous adder structures different heterogeneous adder structures of 16-bit size are to be designed. Different heterogeneous adder architectures are compared with each other in terms of delay (ns) and area (number of LUTs). All the adder structures are designed using VHDL with the help of ISE Xilinx design suite 14.2 and functionally simulated using ISIM simulator. All the designs are to be synthesized using Xilinx XST synthesizer.

KEYWORDS: RCA, CLA, LCSLA, SQRT CSLA, Heterogeneous Adder, Homogeneous Adder, ISE Xilinx Design Suite14.1, ISIM Simulator, XST Synthesizer.

I.INTRODUCTION

In past, the major challenge for VLSI designer is to reduce area of chip by using efficient optimization techniques. Then the next phase is to increase the speed of operation to achieve fast calculations like, in today's microprocessors millions of instructions are performed per second. Speed of operation is one of the major constraints in designing DSP processors. Now, as most of today's commercial electronic products are portable like Mobile, Laptops etc. That requires more battery backup. Therefore, lot of research is going on to reduce power consumption. Therefore, there are three performance parameters on which a VLSI designer has to optimize their design i.e., Area, Speed and Power. It is very difficult to achieve all constraints for particular design, therefore depending on demand or application some compromise between constraints has to be made with some constraints.

Adders are commonly found in the critical path of many building blocks of microprocessors and digital signal processing chips [1], [2]. Adders are essential not only for addition, but also for subtraction, multiplication, and division. Addition is one of the fundamental arithmetic operations. A fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders. The most important for measuring the quality of adder designs in the past were propagation delay, and area. Many different adder architectures have been proposed for speeding up binary addition over the literature survey like RCA, CLA, and CSLA etc [3], [4],[5],[6]. But different adder architectures have some drawbacks in terms of area or delay. As adder forms very important unit in various circuits and systems there is a need to design adder architecture with minimum area without affecting the speed of operation. In this paper various heterogeneous adder architectures are proposed by using different homogeneous adder architectures. Later the designed adders are compared with each other in terms of area (number of LUTs) and delay (ns).

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This paper is structured in brief as Follows-Section II explains about the different homogeneous adder architectures, their operation, advantages and disadvantages. Section III describes the structure and working of heterogeneous adder architecture. The results are explained in section IV i.e. all the designed heterogeneous adder architectures are compared with each other in terms of area (number of LUTs) and delay (ns) . Finally, the paper ends with conclusion.

II. DIFFERENT HOMOGENEOUS ADDER ARCHITECTURES

Ripple carry adder: The ripple carry adder (RCA) is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry [7]. The carryout of one stage is fed directly to the carry-in of the next stage. Even though this is a simple adder and can be used to add unrestricted bit length numbers, it is however not very efficient when large bit numbers are used. One of the most serious drawbacks of this adder is that the delay increases linearly with the bit length. An N-bit RCA is shown in fig 1.

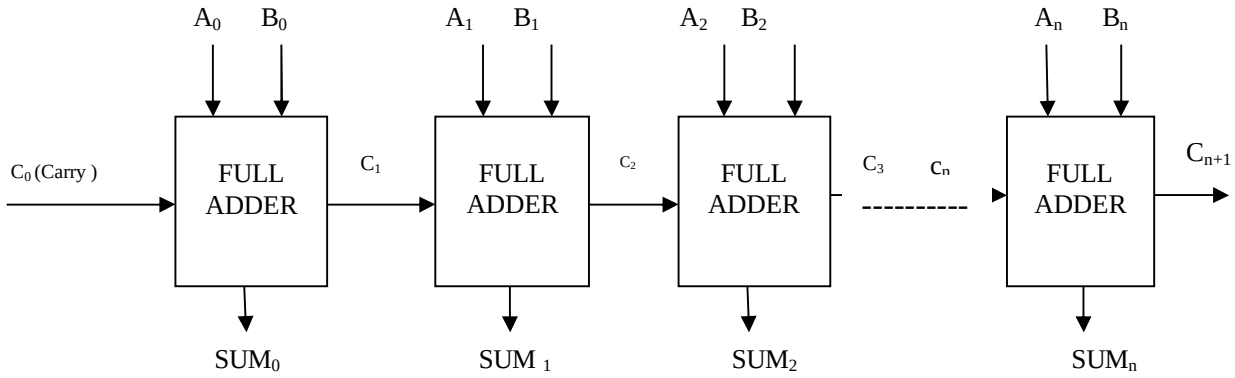

Fig 1. N-bit Ripple carry adder

Carry look ahead adder: Carry look-ahead adder is designed to overcome the latency introduced by the rippling effect of the carry bits. The propagation delay occurred in the parallel adders can be eliminated by carry look ahead adder This adder is based on the principle of looking at the lower order bits of the augends and addend if a higher order carry is generated. This adder reduces the carry delay by reducing the number of gates through which a carry signal must propagate. This adder uses a carry look ahead logic.

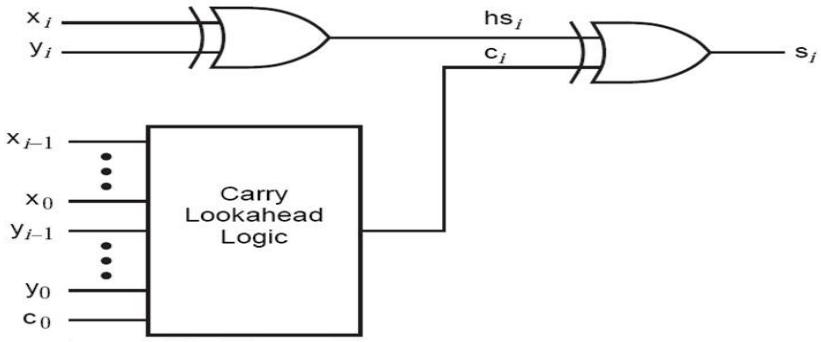

Fig 2. Carry look ahead adder

Carry look ahead depends on two things: Calculating for each digit position, whether that position is going to propagate a carry if one comes in from the right and combining these calculated values to be able to deduce quickly whether, for each group of digits, that group is going to propagate a carry that comes in from the right. The net effect is that the carries start by propagating slowly through each 4-bit group, just as in a ripple-carry system, but then moves 4 times

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faster, leaping from one look ahead carry unit to the next. Finally, within each group that receives a carry, the carry propagates slowly within the digits in that group.

This adder consists of three stages: a propagate block/ generate block, a sum generator and carry generator. The generate block can be realized using the expression

$$G_i = A_i.B_i \text{ for i=0, 1, 2, 3 and so on}$$

Similarly the propagate block can be realized using the expression

$$P_i = A_i \oplus B_i \text{ for i=0, 1, 2, 3and so on}$$

The carry output of the (i-1) th stage is obtained from

$$C_{i(cout)} = G_i + P_iC_{i-1} \text{ for i=0,1,2,3 and so on}$$

The sum output can be obtained by means of

$$S_i = A_i \oplus B_iC_{i-1} \text{ for i=0, 1, 2, 3 and so on.}$$

The disadvantage of carry look ahead adder is the complexity of the carry look ahead circuit in increases as the number of input bits increases and also area increases. So in turn delay of the circuit also increases.

Carry select adder: To solve the carry propagation delay, Carry Select Adder (CSLA) is developed which drastically reduces the area and delay to a great extent [8]. The CSLA is used in many computational systems design to moderate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. A 4-bit carry select adder is shown in fig 3.

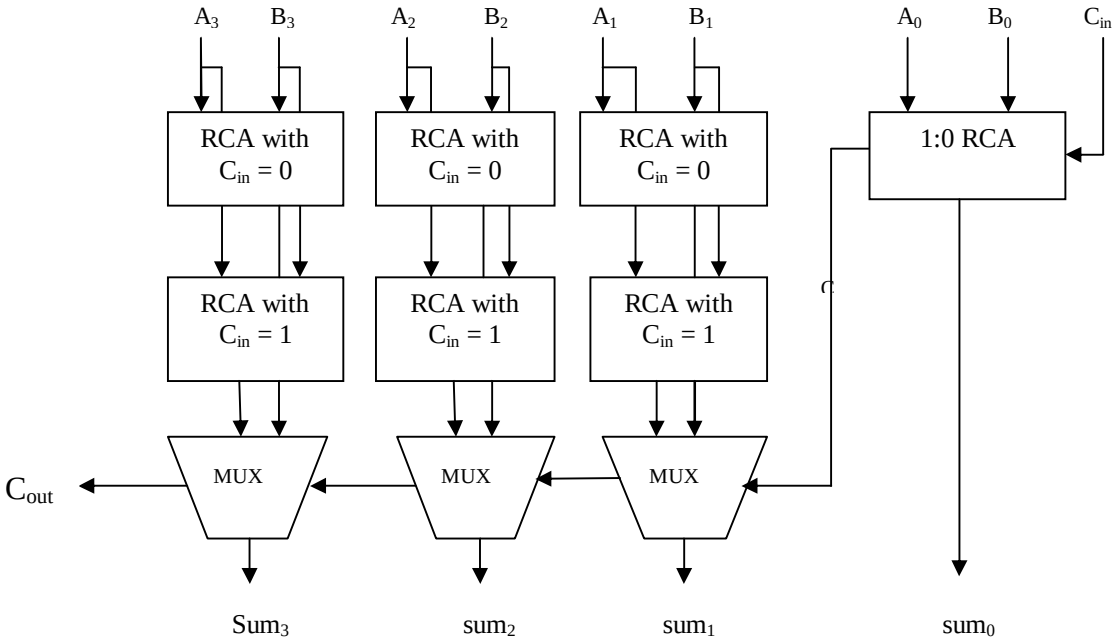

Fig 3. 4-bit carry select adder

Types of carry select adder: There are two types of carry select adders [9]
a. Linear carry select adder (LCSLA)
b. Square root carry select adder (SQRT CSLA).

LCSLA: In linear carry select adder, the input bits to all the carry select stages are equal where as in square root carry select adder the M input bits are divided into $\approx \sqrt{2M}$ carry-select stages.

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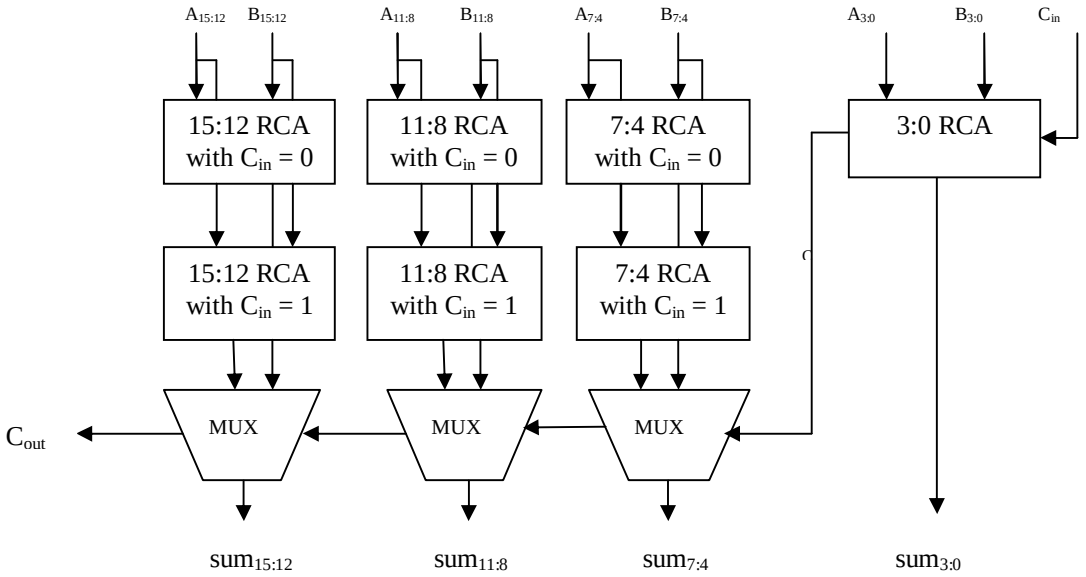

Fig 4. 16-bit Linear CSLA

A linear carry select adder can be constructed by chaining a number of equal length adder stages as shown in figure 4. One can derive the worst case propagation delay of the module. The propagation delay of the adder is again linearly proportional to N. The reason for this linear behavior is that the block select signal that selects between the 0 and 1 solution still has to ripple through all stages in the worst case.

SQRT CSLA: To optimize a design, it is essential to locate the critical timing path first. Consider the case of a 16-bit linear carry-select adder.

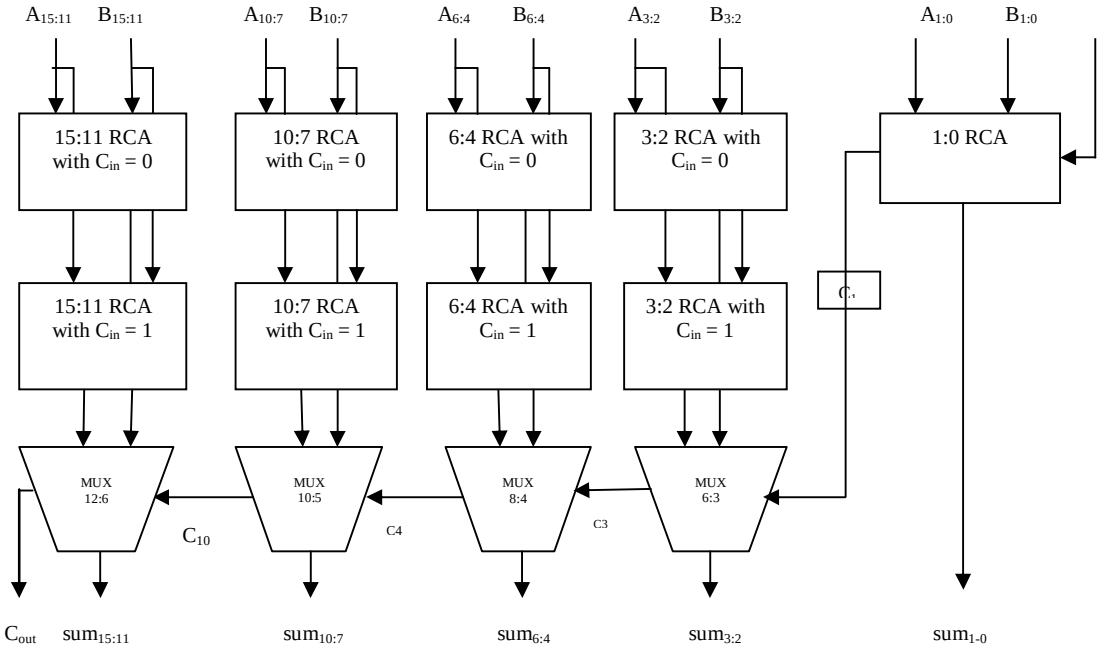

Fig 5. 16-Bit square root CSLA

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To simplify the discussion assume that the full-adder and multiplexer cells have identical propagation delays equal to a normalized value of 1.This analysis demonstrates that the critical path of the adder ripples through the multiplexer networks of the subsequent stage. Consider the multiplexer gate in the last adder stage. The inputs to this multiplexer are the two carry chains of the block and the block-multiplexer signal from the previous stage.

A major mismatch between the arrival times of the signals can be observed. The results of the carry chain are stable long before the multiplexer signal arrives. It makes sense to equalize the delay through both paths. This can be achieved by progressively adding more bits to the subsequent stages in the adder, requiring more time for the generation of the carry signals. For example, the first stage can add 2 bits, the second contains 3, the third has 4, and so forth. This type of adder is called square root carry select adder

The four adders i.e. RCA, CLA, LCSLA and SQRT CSLA[10] are designed for various input bit size and also synthesized using Xilinx ISE 14.2 EDA tool. After synthesis process, the designer can obtain the synthesis report which give information on area utilization of the design on the selected FPGA type, delay report, various timing reports and many more reports. Table illustrates the comparison of all the designed four adders in terms of delay (ns).

Adder structure	Delay (ns)	Area(number of LUTs)
16-bit RCA	24.68	32
16-bit CLA	23.34	27
16-bit LCSLA	19.09	47
16-bit SQRT CSLA	18.46	46

Table 1. Comparison of four adder structures in terms of delay (ns) and Area (number of LUTs)

From table 1, it is clear that the SQRT CSLA is faster when compared with the other three adders. As shown in table, 16- bit SQRT CSLA has 18.46 ns delay to output the result whereas the remaining has- RCA has 24.68 ns, CLA 23.34 ns and LCSLA has 19.09 ns delay to output the result.

III. HETEROGENEOUS ADDER ARCHITECTURE

Different 16-bit Heterogeneous adder designs are proposed in this paper which consists of four sub adders RCA,CLA,LCSLA and SQRT CSLA. All these four sub adders are concatenates to form a 16-bit heterogeneous adder. The order i.e. bit-width of each sub adder has an impact on the performance of a heterogeneous adder.

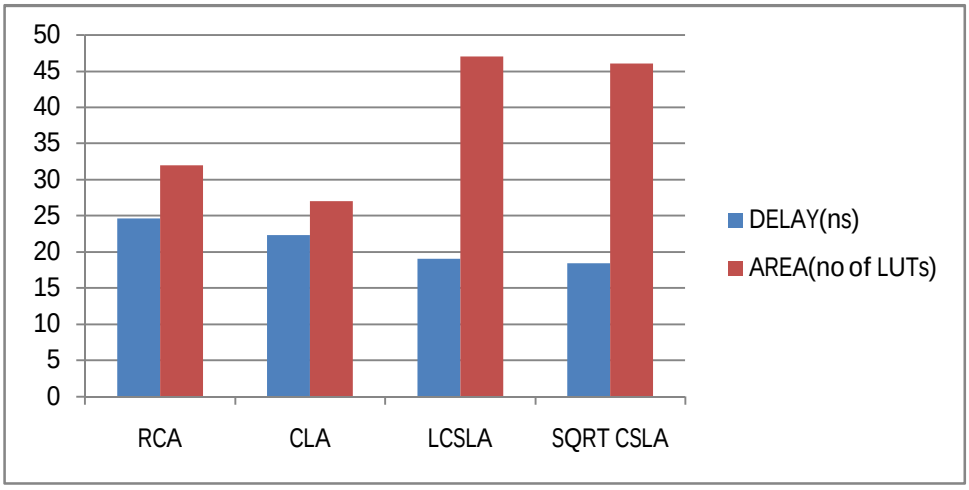

Fig 6. Delay Area comparison graph for different Homogeneous Adders

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Now, the main point of consideration is that how to select number of bits for each sub-adder. Bit-width selection for each sub-adder can be done on the basis of requirements (i.e. Area, Speed and Power constraints) of particular application where the design is to be implemented. However, with the help of heterogeneous adder architecture, any desired performance can be achieved by adjusting bit-width of sub-adders.

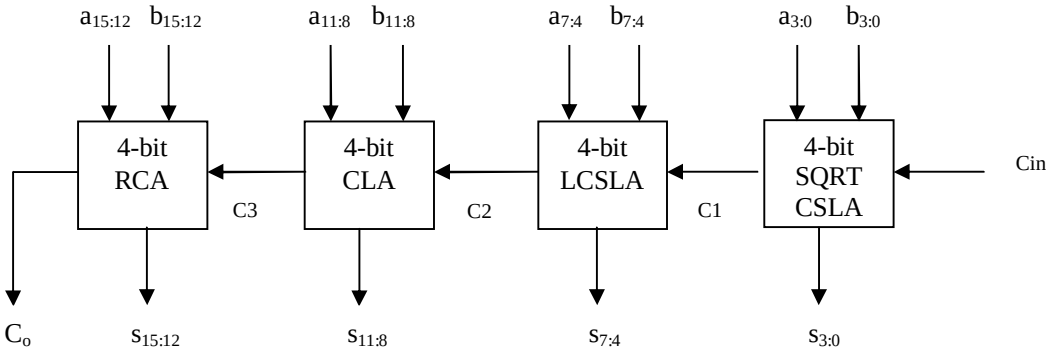

Fig 7. 4-bit SQRT CSLA+ 4-bit LCSLA+ 4-bit CLA+ 4-bit RCA heterogeneous adder

Figure 7 shows a heterogeneous adder architecture consisting of RCA, CLA, LCSLA and SQRT CSLA of size 4-bit. The lower 4 bit input i.e., 0 to 3 bits and carry input are applied to SQRT CSLA. Whereas the 4-bits i.e., 4 to7 bits is applied to LCSLA and the 4-bits i.e., 8to 11 bits applied to CLA and the lower 4 bits i.e., 12 to 15 is applied to RCA. The carry input to LCSLA block is the carry output of SQRT CSLA block and the carry input to CLA block is the carry output of LCSLA block and the carry input to RCA block is the carry output of CLA. The SQRT CSLA block generates the lower 4 bit sum output i.e., 0 to 3 bits whereas LCSLA produces 4 bits sum output i.e., 4 to 7 bits and CLA block produces 4 bits sum output i.e., 8 to 11 and RCA produces higher 4 bits sum output i.e., 12 to 15 bits and carry output of the adder. In the same manner different heterogeneous adder architectures are proposed in this paper which consists of different homogeneous adder architectures of different bit size.

IV. SIMULATION AND SYNTHESIS RESULT

The different heterogeneous adders are designed for 16 bit size using VHDL[11]. Functional simulations are carried out by using Xilinx 14.2 ISE ISIM simulator.

Heterogeneous Adder type	Delay (ns)	Area(no of LUTs)
4CLA+12LCSLA	20.828	41
8RCA+8SQRT CSLA	21.78	40
4RCA+8SQRT CSLA+4CLA	21.7	36
4LCSLA+12SQRT CSLA	22.6	39
8LCSLA+8SQRT CSLA	22.7	37
1RCA+8SQRT CSLA+4LCSLA+3CLA	22.823	37
4SQRT CSLA+4LCSLA+4CLA+4RCA	23.45	32
4RCA+8LCSLA+4CLA	23.424	31
8RCA+4LCSLA+4CLA	23.504	31
12RCA+4CLA	23.732	31
8CLA+4SQRT CSLA+4LCSLA	24.4	32
8RCA+8LCSLA	24.510	32
2RCA+4LCSLA+4SQRT CSLA+6CLA	24.5	33
8RCA+8CLA	24.6	32

Table 2. Comparison of different heterogeneous adders in terms of delay (ns) and Area (number of LUTs)

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The adder designs are synthesized using XST synthesizer provided by Xilinx 14.2[12]. Table 2 illustrates the comparison of all the designed adders in terms of delay (ns) and area (number of LUTs).It is a synthesis tool from Xilinx. It provides area report and delay report of the design in terms of number of LUTs and in nano seconds respectively. From the above table 2, it is clear that as the delay is decreasing the area is increasing and also as the area is decreasing the speed is increasing. So it can be said that the area and speed are inversely related to each other. As shown in table 2, 4CLA+12LCSLA adder is having the least delay i.e., 20.828(ns) but it is occupying more number of LUTs i.e., 41 when compared to other designed heterogeneous adders. Also 8RCA+8CLA adder is occupying less number of LUTs i.e., 32 when compared to others but its delay is 24.6 ns which is very high when compared with other adders.

V. CONCLUSION

In this paper, different types of heterogeneous adders are designed using different types of adders like RCA, CLA, LCSLA and SQRT CSLA. As shown in table 2, 4-bit CLA +12-bit LCSLA adder is having minimum delay compared to other adder topologies but it has occupied more number of LUTs. At the same time, 8-bit RCA+8-bit CLA has occupied less number of LUTs, but delay is increased. So it can be concluded that 4-bit CLA+12-bit LCSLA adder is the best adder compared to other adder topologies in terms of speed and 8-bit RCA+8-bit CLA is best adder in terms of area when compared with other designed adders in terms of area i.e., number of LUTs occupied. So the 4-bit CLA+12-bit LCSLA adder be used for high speed applications and 8-bit RCA+8-bit CLA adder is used in applications where low area and low power consumption is required. Finally it is concluded that the area and speed are inversely related to each other i.e., as area increases speed decreases and vice versa. Depending the need of application i.e., area, power and speed requirement the type of adder to be used can be selected.

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