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Design and Validation of threshold Model Using BSIM3v 3.2.2

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***Abstract*:** This paper presents a BSIM3v3.2.2 threshold model validation using SPICE simulations and mathematical models of BSIM are computed using MATLAB simulation and comparison between the mathematical and simulation model is presented. Further the short channel and narrow channel effects are analyzed and effect on threshold voltage is investigated.

Keywords: Threshold, Narrow channel, short channel, Threshold.

I. INTRODUCTION

The threshold voltage, commonly abbreviated as V_{th}, of a MOSFET is usually defined as the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. An accurate modelling of the threshold voltage is one of the most important requirements for precise description of device electrical characteristics. It also serves as a useful reference point for the evaluation of device operation regimes. By using threshold voltage, the whole device operation regime can be divided into three operational regions. Reverse short-channel effect (RSCE) is a result of non-uniform channel doping (halo doping) in modern processes[1]. And helps in controlling the threshold voltage. First, if the gate voltage is greater than the threshold voltage, the inversion charge density is larger than the substrate doping concentration and MOSFET is operating in the strong inversion region and drift current is dominant.

Second, if the gate voltage is smaller thanV_{th}, the inversion charge density is smaller than the substrate doping concentration. The transistor is considered to be operating in the weak inversion (or sub threshold) region where diffusion current is now dominant [2 -7]. Lastly, if the gate voltage is very close toV_{th}, the inversion charge density is close to the doping concentration and the MOSFET is operating in the transition region. As the channel length of MOSFETs is scaled down to deep-sub micrometer or sub-180 nm regime, short-channel effects, such as, steep threshold voltage roll-off, increased off-state leakage current and bulk punch through have been observed [2].

In this work threshold voltage dependence investigated over Doping concentration (uniform & Non uniform), Short Channel effect and Narrow Channel effect [8] and detailed analysis of device is targeted with number of device parameters.

The paper is organized as section II presents previous model used by BSIM v.3.3 and in section III results are formulated and finally conclusion.

II. BSIM THRESHOLD MODEL

For MOSFET's with long channel length/width and uniform substrate doping concentration V_{th} is given by [8]:

$$V_{th} = V_{fb} + \phi_s + \gamma(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s}$$

And

$$V_{th} = V_{tideal} + \gamma(\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s} \tag{1}$$

Where V_{fb} is the flat band voltage and V_{tideal} is the threshold voltage of the long channel device at zero substrate bias and γ is the body bias coefficient and is given by:

$$\gamma = \frac{\sqrt{2\epsilon_{si} q N_a}}{\mathrm{C_{ox}}} \tag{2}$$

where N_a is the substrate doping concentration. The surface potential is given by:

$$\phi_\mathrm{s} = 2\frac{K_b T}{q}\ln(\frac{N_a}{n_i}) \tag{3}$$

Equation (2.1) assumes that the channel is uniform and makes use of the one dimensional Poisson equation in the vertical direction of the channel. This model is valid only when the substrate doping concentration is constant and the channel length is long. Under these conditions, the potential is uniform along the channel.

(a) Vertical non-uniform doping effect

Modifications have to be made when the substrate doping concentration is not uniform and/or when the channel length is short, narrow, or both. Then the threshold model in (1) will become:

$$V_{th} = V_{tideal} + \mathrm{K}_1(\sqrt{\phi_\mathrm{s} - \mathrm{V_{bs}}} - \sqrt{\phi_\mathrm{s}}) - K_2\mathrm{V_{bs}} \tag{4}$$

The distribution of impurity atoms inside the substrate is approximately a half Gaussian distribution

K_1 and K_2 can be determined by the criteria that $\mathrm{V_{th}}$ and its derivative versus $\mathrm{V_{bs}}$ should be the same at $\mathrm{V_{bm}}$, where $\mathrm{V_{bm}}$is the maximum substrate bias voltage. Therefore, using equations (2.1) and (2.4), $K1$ and $K2$ [3] will be given by the following:

$$K_1 = \gamma_2 - 2K_2\sqrt{\phi_\mathrm{s} - \mathrm{V_{bm}}} \tag{5}$$

$$K_2 = \frac{(\gamma_1-\gamma_2)(\sqrt{\phi_s-}\mathrm{V_{bx}}-\sqrt{\phi_s})}{2\sqrt{\phi_s}(\sqrt{\phi_s-}\mathrm{V_{bm}}-\sqrt{\phi_s})+V_{bm}} \tag{6}$$

where γ_1 and γ_2 are body bias coefficients when the substrate doping concentration are equal to $\mathrm{N_{ch}}$ and $\mathrm{N_{sub}}$, respectively:

$$\gamma_1 = \frac{\sqrt{2\epsilon_\mathrm{si}\mathrm{qN_{ch}}}}{\mathrm{C_{ox}}} \tag{7}$$

$$\gamma_2 = \frac{\sqrt{2\epsilon_\mathrm{si}\mathrm{qN_{sub}}}}{\mathrm{C_{ox}}} \tag{8}$$

$\mathrm{V_{bx}}$is the body bias when the depletion width is equal to $\mathrm{X_t}$. Therefore, $\mathrm{V_{bx}}$ satisfies:

$$\frac{\mathrm{qN_{ch}\,X_t}^2}{2\epsilon_\mathrm{si}} = \phi_\mathrm{s} - \mathrm{V_{bx}} \tag{9}$$

(b) Lateral non-uniform doping effect

For some technologies, the doping concentration near the source/drain is higher than that in the middle of the channel. This is referred to as lateral non-uniform doping. As the channel length becomes shorter, lateral non-uniform doping will cause

$\mathrm{V_{th}}$ to increase in magnitude because the average doping concentration in the channel is larger. The average channel doping concentration can be calculated as

$$N_{eff} = N_a(1 + \frac{NLX}{L}) \qquad (10)$$

Due to the lateral non-uniform doping effect, (4) becomes:

$$\mathrm{V_{th} = V_{th0} + K_1\sqrt{\phi_s - V_{bs}} - K_2V_{bs} + K_1\left(\sqrt{1 + \frac{NLX}{L_{eff}}} - 1\right)\sqrt{\phi_s}} \qquad (11)$$

This effect gets stronger at a lower body bias.

(c) *Short Channel Effect*

A MOS transistor is called a short-channel device if its channel length is on the same order of magnitude as the depletion region thicknesses of the source and drain junctions. Alternatively, a MOSFET can be defined as a short-channel device if the effective channel length $\mathrm{L_{eff}}$ is approximately equal to the source and drain junction depthX_j. The short-channel effects that arise in this case are attributed to two physical phenomena:

(i) The limitations imposed on electron drift characteristics in the channel,

(ii) The modification of the threshold voltage due to the shortening channel length.

The threshold voltage of a long channel device is independent of the channel length and the drain voltage. Its dependence on the body bias is given by (4). However, as the channel length becomes shorter, the threshold voltage shows a greater dependence on the channel length and the drain voltage. The dependence of the threshold voltage on the body bias becomes weaker as channel length becomes shorter, because the body bias has less control of the depletion region. The short-channel effect is included in the V_{th} model as

$$V_{th} = V_{th0} + \mathrm{K_1}(\sqrt{\mathrm{\phi_s - V_{bs}}} - \sqrt{\mathrm{\phi_s}})\text{-}K_2\mathrm{V_{bs}} + \mathrm{K_1}\sqrt{(1 + \frac{\mathrm{NLX}}{\mathrm{L_{eff}}} - 1)}\sqrt{\mathrm{\phi_s}} - \Delta\mathrm{V_{th}} \qquad (12)$$

where $\Delta\mathrm{V_{th}}$ is the threshold voltage reduction due to the short channel effect.

$$\Delta\mathrm{V_{th}} = \theta_{\mathrm{th}}(\mathrm{L})(2(\mathrm{V_{bi}} - \phi_s) + \mathrm{V_{ds}}) \qquad (13)$$

Many models have been developed to calculate$\Delta\mathrm{V_{th}}$. This quasi-2D model concluded that:

$$\Delta\mathrm{V_{th}(V_{ds})} = \theta_{\mathrm{dibl}}(\mathrm{L})((\mathrm{E_{ta0}} + \mathrm{E_{tab}V_{bs}})\mathrm{V_{ds}} \qquad (14)$$

(d) Narrow Channel Effect

Earlier, we have analysis the effect of Length that’s get short is referred to as short channel effect and now after the short channel the narrow channel effect is considered that is the width of the devices are getting narrow. Considering the NMOS device the actual depletion region in the channel is always larger than what is usually assumed under the one-dimensional analysis due to the existence of fringing fields [2]. This effect becomes very substantial as the channel width decreases and the depletion region underneath the fringing field becomes comparable to the "classical" depletion layer formed from the vertical field. The net result is an increase in $\mathrm{V_{th}}$.

$$V_{th} =$$

$$V_{th0ox} + K_{1ox}\sqrt{\phi_s - V_{bseff}} - K_{2ox}V_{bseff} + K_{1ox}\left(\sqrt{1 + \frac{NLX}{L_{eff}}} - 1\right)\sqrt{\phi_s}(K_3 + K_{3b}V_{bs})\frac{T_{ox}}{W'_{eff} + W_0}\phi_s -$$

$$D_{vt0w}\left(exp\left(-D_{vt1w}\frac{W'_{eff}L_{eff}}{2\,l_{tw}}\right)+2exp\left(D_{vt1w}\frac{W'_{eff}\,L_{eff}}{l_{tw}}\right)\right)(V_{bi}-\phi_s)-D_{vt0}\left[exp\left(\frac{-D_{vt1}L}{2\,l_t}\right)+2\,exp\left(-\frac{D_{vt1}L}{l_t}\right)\right](V_{bi}-\phi_s)-\ [exp\left(\frac{-D_{sub}L}{2\,l_{to}}\right)+2\,exp\left(-\frac{D_{sub}L}{l_{to}}\right)]((E_{ta0}+E_{tab}V_{bseff})V_{ds}) \quad (15)$$

III. RESULT & DISCUSSION

The above approximated model is validated by using 180nm CMOS process parameters. Length and width of the device is taken as 180 nm and 270 nm and the temperature on which the device simulation is done i.e. 300 K. The supply voltage V_{DD} is 1.8v and the gate to source input voltage maximum limit is set to 1.8v. And the DC analysis of the NMOS device is performed on the SPICE EDA tool. Figure 1 shows the schematic of NMOS used for simulation.

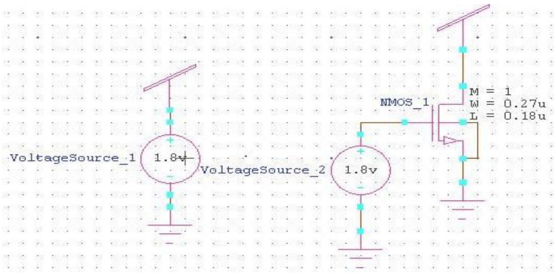

Figure 1 Schematic of NMOS

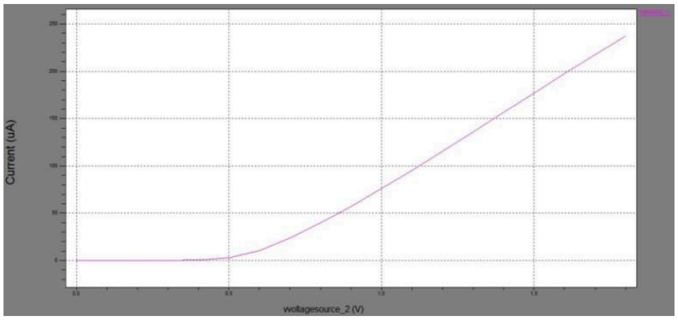

Fig. 2 The output waveform of NMOS device

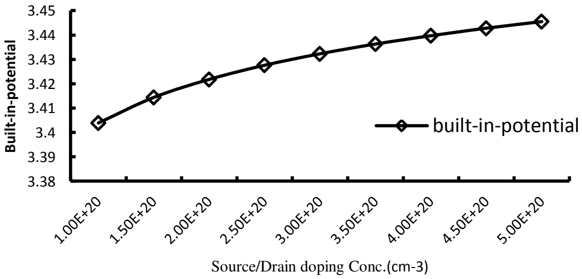

Figure 3 Built-in-potential versus source/drain doping

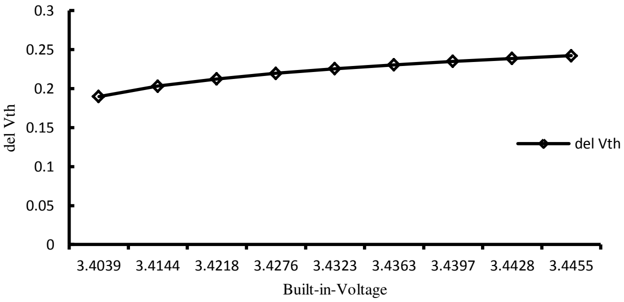

Figure 4. Shows the ΔV_{th} (delVth) versus built-in-potential

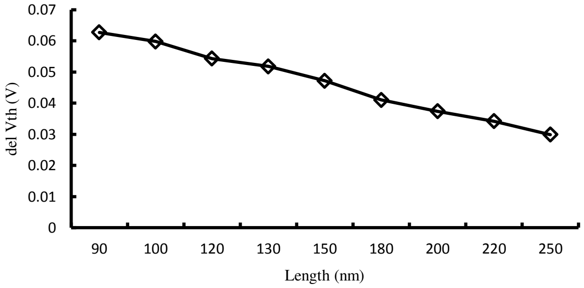

Figure 5. ΔV_{th} versus the length (nm) at Channel doping conc. of 2.8469e-18 cm-3

The threshold voltage which is calculated by the SPICE and MATLAB simulator is shown in table 1. And is highlighted by yellow mark. And no of parameters used by MATLAB simulator is detailed in table 2. (with the default values of BSIM and used in this work). Figure 2 shows the threshold voltage at which NMOS device is ON.

The above figure 3 reflects the effect on the built-in-potential (V_{bi}) versus source/drain doping concentration (N_d) [8].

And ΔV_{th} is the threshold voltage reduction due to the short channel of the device. Now considering the variation in ΔV_{th} with respect to the built-in-Voltage. The relation between the ΔV_{th} and the built-in-Voltage is given by the (13) and relation between V_{bi} and ΔV_{th} is validated as shown in figure 4.

If the parameter in the equation (13) are remain constant and the built-in-Voltage vary according to the formulation they are directly related to each other as built-in-Voltage increases the ΔV_{th} increases and similarly if the built-in-Voltage decrease the ΔV_{th} will decrease. Further w.r.t. to length of device the BSIM model is validated.The parameter Length is the major parameter in the sub-micron technology as the technology moving toward the sub-micron the Length of the device getting shorter so the impact of the length on the ΔV_{th} is expressed graphically in figure 5.

The ΔV_{th} is the function of length according to the equation (13) that means the ΔV_{th} depend upon the length as the length of the device is increases the ΔV_{th} will decrease. One major consideration is that the channel doping concentration is 2.8469e-18cm-3.

IV.CONCLUSION

Based on device parameters approximation the mathematical models of BSIM3v3.2.2 threshold model is validated with the SPICE simulations. The threshold voltage calculated is 0.436V and it is 98% close to the simulated model. Scaling effect is also investigated in terms of short Channel Effect. And the increase in the length the ΔV_{th} is increased and resulted threshold voltage is decreased.

Further it is also concluded that the first order coefficient of the Narrow channel shows the decrease in the threshold voltage but the second coefficient and has a negligible effect on the threshold voltage. This work will help to the users of VLSI modelling i.e how to work with 49 and 57 Level MOS parameters.

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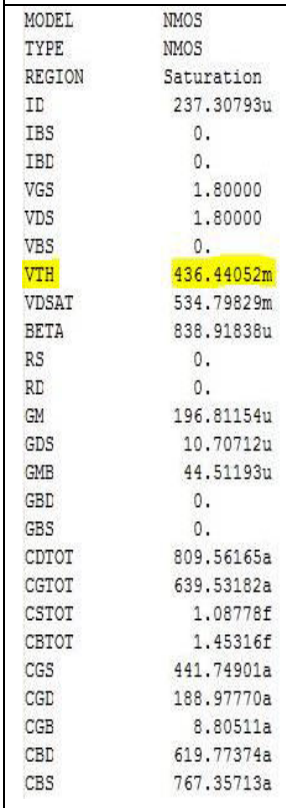
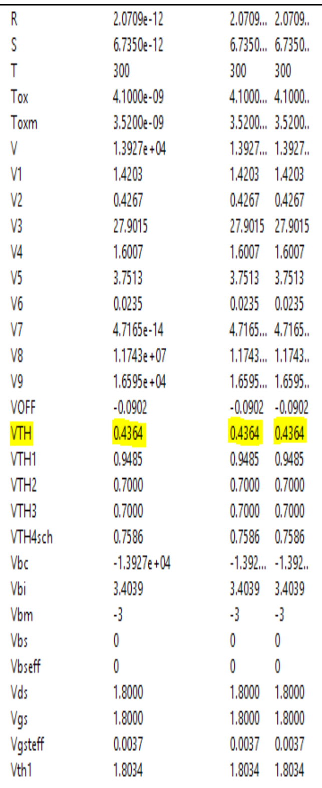
Table 1. Threshold voltage calculation.

SIMULATED
Threshold Voltage(mV)



```
MODEL         NMOS
TYPE          NMOS
REGION        Saturation
ID              237.30793u
IBS               0.
IBD               0.
VGS               1.80000
VDS               1.80000
VBS               0.
VTH             436.44052m
VDSAT           534.79829m
BETA            838.91838u
RS                0.
RD                0.
GM              196.81154u
GDS              10.70712u
GMB              44.51193u
GBD               0.
GBS               0.
CDTOT           809.56165a
CGTOT           639.53182a
CSTOT             1.08778f
CBTOT             1.45316f
CGS             441.74901a
CGD             188.97770a
CGB               8.80511a
CBD             619.77374a
CBS             767.35713a
```

CALCULATED
Threshold Voltage(V)



```
R         2.0709e-12    2.0709...  2.0709..
S         6.7350e-12    6.7350...  6.7350..
T         300           300        300
Tox       4.1000e-09    4.1000...  4.1000..
Toxm      3.5200e-09    3.5200...  3.5200..
V         1.3927e+04    1.3927...  1.3927..
V1        1.4203        1.4203     1.4203
V2        0.4267        0.4267     0.4267
V3        27.9015       27.9015    27.9015
V4        1.6007        1.6007     1.6007
V5        3.7513        3.7513     3.7513
V6        0.0235        0.0235     0.0235
V7        4.7165e-14    4.7165...  4.7165..
V8        1.1743e+07    1.1743...  1.1743..
V9        1.6595e+04    1.6595...  1.6595..
VOFF      -0.0902       -0.0902    -0.0902
VTH       0.4364        0.4364     0.4364
VTH1      0.9485        0.9485     0.9485
VTH2      0.7000        0.7000     0.7000
VTH3      0.7000        0.7000     0.7000
VTH4sch   0.7586        0.7586     0.7586
Vbc       -1.3927e+04   -1.392...  -1.392..
Vbi       3.4039        3.4039     3.4039
Vbm       -3            -3         -3
Vbs       0             0          0
Vbseff    0             0          0
Vds       1.8000        1.8000     1.8000
Vgs       1.8000        1.8000     1.8000
Vgsteff   0.0037        0.0037     0.0037
Vth1      1.8034        1.8034     1.8034
```

Table 2.
The TSMC 180 nm parameter is used in the analyses which are shown:

Symbols used in Equation	**Symbol used in SPICE**	**Descriptions**	**Default**	**Used**
Vth0	vth0	Threshold voltage @Vbs=0 for Large L.	0.7	0.3796589
VFB	Vfb	Flat-band voltage	Calculated	-1.0
K1	K1	First order body effect coefficient	0.5	0.5935169
K2	K2	Second order body effect coeff.	0.0	2.38533E-3
K3	K3	Narrow width coefficient	80.0	1E-3
K3b	K3b	Body effect coefficient of k3	0.0	3.1905105
W0	W0	Narrow width parameter	2.5e-6	1E-7
Nlx	Nlx	Lateral non-uniform doping Parameter	1.74e-7	1.786849E-7
Vbm	Vbm	Maximum applied body bias in Vth calculation	-3.0	-3.0
Dvt0	dvt0	first coefficient of short-channel effect on Vth	2.2	1.7203781
Dvt1	dvt1	Second coefficient of short channel effect on Vth	0.53	0.4308344
Dvt2	dvt2	Body-bias coefficient of short channel effect on Vth	-0.032	0.0467521
Dvt0w	dvt0w	First coefficient of narrow width effect on Vth for small channel length	0	0
Dvt1w	dvtw1	Second coeff. of narrow width effect on Vth for small channel length	5.3e6	0
Symbols used in Equation	Symbol used in SPICE	Descriptions	Default	Used
Dvt2w	dvt2w	Body-bias coefficient of narrow width effect for small channel length	-0.032	0
µ0	u0	Mobility at Temp = Tnom NMOSFET PMOSFET	670.0 250.0	269.0635418
Ua	Ua	First-order mobility degradationCoeff.	2.25e-9	-1.188565E-9
Ub	Ub	Second-order mobility degradation oeff.	5.87e-19	1.930877E-18
Uc	Uc	Body-effect of mobility degradation Coefficient	mobMod=1,2:-4.56e-11, mobMod=3:-0.046	2.224818E-11
Vsat	Vsat	Saturation velocity at Temp =Tnom	8.0e4	9.67502E4
A0	a0	Bulk charge effect coefficient	1.0	2

		for channel length		
Ags	Ags	gate bias coefficient of Abulk	0.0	0.4169677
B0	b0	Bulk charge effect coefficient for channel width	0.0	-1.063955E-8
B1	b1	Bulk charge effect width offset	0.0	-1E-7
Keta	Keta	Body-bias coefficient of bulkcharge effect	-0.047	-7.704208E-3
A1	a1	First non-saturation effect Parameter	0.0	7.99632E-4
A2	a2	Second non-saturation factor	1.0	0.999873
Rdsw	Rdsw	Parasitic resistance per unit Width	0.0	105
Symbols used in Equation	**Symbol used in SPICE**	**Descriptions**	**Default**	**Used**
Prwb	Prwb	Body effect coefficient of Rdsw	0	-0.2
Prwg	Prwg	Gate bias effect coefficient of Rdsw	0	0.5
Wr	Wr	Width Offset from Weff for Rds calculation	1.0	1
Wint	Wint	Width offset fitting parameter from I-V without Bias	0.0	2.025957E-9
Lint	Lint	Length offset fitting parameter from I-V without Bias	0.0	1.028309E-8
dWg	Dwg	Coefficient of Weff's gate Dependence	0.0	-6.4982E-10
dWb	Dwb	Coefficient of Weff's substrate body bias dependence	0.0	1.217904E-8
Voff	Voff	Offset voltage in the sub-threshold region at large W and L	-0.08	-0.0901723
Nfactor	Nfactor	Sub-threshold swing factor	1.0	2.3820479
Eta0	eta0	DIBL coefficient in sub-threshold Region	0.08	1.448044E-3
Etab	Etab	Body-bias coefficient for the sub-threshold DIBL effect	-0.07	-2.754731E-4
Dsub	Dsub	DIBL coefficient exponent in Sub-threshold	Drout	0.0110906
Symbols used in	Symbol used in	Descriptions	Default	Used

Equation	SPICE			
Cdscd	Cdscd	Drain-bias sensitivity of Cdsc	0.0	0
Pclm	Pclm	Channel length modulation Parameter	1.3	= 1.0622551
Pdiblc1	pdiblc 1	First output resistance DIBL effect correction parameter	0.39	0.3172281
Pdiblc2	pdiblc 2	Second output resistance DIBL effect correction parameter	0.0086	3.755701E-3
Pdiblcb	Pdiblcb	Body effect coefficient of DIBL correction parameters	0	-0.1
Drout	Drout	L dependence coefficient of the DIBL correction parameter in Rout	0.56	0.783102
Pscbe1	pscbe1	First substrate current bodyeffectparameter	4.24e8	5.995957E10
Pvag	Pvag	Gate dependence of Early voltage	0.0	0.3568363
δ	Delta	Effective Vds parameter	0.01	0.01
Cit	Cit	Interface trap capacitance	0.0	0
Cdsc	Cdsc	Drain/Source to channel coupling Capacitance	2.4e-4	2.4E-4
Cdscb	Cdscb	Body-bias sensitivity of Cdsc	0.0	0
Xpart	Xpart	Charge partitioning flag	0.0	0.5
CGS0	Cgso	Non LDD region source-gate overlap capacitance per channel length	Calculated	7.45E-10
CGD0	Cgdo	Non LDD region drain-gate overlap capacitance per channel length	Calculated	7.45E-10
Symbols used in Equation	**Symbol used in SPICE**	**Descriptions**	**Default**	**Used**
CGB0	Cgbo	Gate bulk overlap capacitance per unit channel length	0.0	1E-12
Cj	Cj	Bottom junction capacitance per unit area at zero bias	5.0e-4	9.725136E-4
Mj	Mj	Bottom junction capacitance grating coefficient	0.5	0.3610145
Mjsw	Mjsw	Source/Drain side wall junction capacitance grading coefficient	0.33	0.1
Cjsw	Cjsw	Source/Drain side wall junction capacitance per unit area	5e-10	2.269386E-10
Cjswg	Cjswg	Source/drain gate side wall junction capacitance grading Coefficient	Cjsw	3.3E-10
Mjswg	Mjswg	Source/drain gate side wall junction capacitance grading Coefficient	Mjsw	0.1
Pbsw	Pbsw	Source/drain side wall junction built-in	1.0	0.6351005

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		potential		
Pb	Pb	Bottom built-in potential	1.0	0.7292509
Pbswg	Pbswg	Source/Drain gate side wall junction built-in potential	Pbsw	0.6351005
Cf	Cf	fringing field capacitance	Calculated	0
Wl	Wl	Coefficient of length dependence for width offset	0.0	0
Wln	Wln	Power of length dependence of width offset	1.0	1
Ww	Ww	Coefficient of width dependence for width offset	0.0	0
Symbols used in Equation	**Symbol used in SPICE**	**Descriptions**	**Default**	**Used**
Wwn	Wwn	Power of width dependence of width offset	1.0	1
Wwl	Wwl	Coefficient of length and width cross term for width offset	0.0	0
Ll	Ll	Coefficient of length dependence for length offset	0.0	0
Lln	Lln	Power of length dependence for length offset	1.0	1
Lw	Lw	Coefficient of width dependence for length offset	0.0	0
Lwn	Lwn	Power of width dependence for length offset	1.0	1
Lwl	Lwl	Coefficient of length and width cross term for length offset	0.0	0
Tox	Tox	Gate oxide thickness	1.5e-8	4.1E-9
Toxm	Toxm	Tox at which parameters are extracted	Tox	27
Xj	Xj	Junction Depth	1.5e-7	1E-7
γ1	gamma1	Body-effect coefficient near the Surface	Calculated	
γ2	gamma2	Body-effect coefficient in the Bulk	Calculated	
Nch	Nch	Channel doping concentration	1.7e17	2.3549E17
Nsub	Nsub	Substrate doping concentration	6e16	0.0110906
Vbx	Vbx	Vbs at which the depletion region width equals xt	Calculated	
Xt	Xt	Doping depth	1.55e-7	1.55e-7