Design and Implementation of Hybrid SET-CMOS 4-to-1 MUX and 2-to-4 Decoder Circuits

N. Basanta Singh

Associate Professor, Department of Electronics & Communication Engineering, Manipur Institute of Technology, Imphal-795004, India

ABSTRACT: Single Electron Transistor (SET) is an attractive technology for future low power VLSI/ULSI systems. SET has high integration density and ultra-low power consumption. However, Single electron transistors have extremely poor driving capabilities so that direct application to practical circuits is as yet almost impossible. An approach to overcome this problem is to build hybrid circuits of SETs and CMOS. In this work, hybrid SET-CMOS 4-to-1 MUX and 2-to-4 Decoder are designed and implemented. The MIB compact model for SET device and BSIM4.6.1 model for CMOS are used. All the circuits are verified by means of T-Spice simulation software.

 Keywords: Single Electron Transistor, CMOS, Hybrid CMOS-SET Circuits, MIB, T-Spice, 4-to-1 MUX and 2-to-4 Decoder.

I. INTRODUCTION

   Single Electron Transistor is an attractive candidate for future ultra low power VLSI and ULSI systems. However, practical SET circuit applications are likely not feasible with a pure Single Electronics approach, mainly due to its low current drive. And also it is unlikely that SET can replace the CMOS technology. However, the unique properties such as Coulomb blockade oscillations of SETs can be exploited to increase CMOS functionalities by hybrid CMOS-SET approach. By combining SET and CMOS, and exploiting the Coulomb Blockade oscillation phenomenon of SET and high current drive facility of CMOS, one can bring out new functionalities which are very difficult to implement by pure CMOS approach.

   Single electronics implies the possibility to control the movement and position of a single electron or a small amount of electrons [1]. Single-electron transistors (SETs) are three-terminal switching devices which consist of a small conducting island coupled to source and drain leads by tunnel junctions and capacitively coupled to one or more gates. The first experimental SETs were fabricated by Fulton and Dolan [2] and Kuzmin and Likharev [3] in 1987. SET is expected to be a key device for future VLSI/ULSI circuit implementation because of its low power dissipation, small size and highly functional features [1, 4]. The real problems preventing the use of SETs in most applications are their low current drivability, small voltage gain, high output impedance, and high sensitivity to background charges [5-9]. Since CMOS devices have advantages that can compensate for the drawbacks of SETs, hybrid SET-CMOS circuits that combine both SET and CMOS devices is one of the possible solutions to the problems of SET mentioned above.

   In this work, hybrid SET-CMOS 4-to-1 MUX and 2-to-4 Decoder circuits are designed and implemented. The operation of the proposed circuits are analyzed and verified in Tanner environment. The MIB compact model for SET devices and BSIM4.6.1 model for CMOS are used.

II. THEORY

   The main device of the Single Electron technology is the tunnel junction through which individual electron can move in a controlled manner [10]. Their operation is based on the Coulomb blockade [11]. A schematic structure and symbol of a tunnel junction are shown in Fig. 1. It can be considered as two conductors separated by a thin layer of insulating material.

Electrons are considered to tunnel through a tunnel junction one after another [12- 14]. The required threshold voltage across the tunnel junction to make a tunnel event possible, known as known as the critical voltage V_c, can be calculated with the equation [13]

$$V_c = \frac{e}{2(C_e + C_T)} \qquad (1)$$

Where e = 1.602 x 10^{-19} C, C_T is the junction capacitance and C_e is the equivalent capacitance for remainder circuit as viewed from the tunnel junction's perspective.
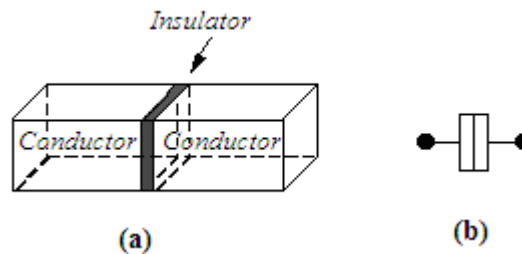

Fig. 1. Tunnel Junction: (a) Schematic Structure and (b) Symbol

The simplest functional single-electron device is a single-electron box [3]. The equivalent circuit of a single-electron box is shown in Fig 2. It is composed of a quantum dot connected with two electrodes. One electrode, called the source electrode, is connected with the quantum dot through a tunnel junction and the other electrode, called the gate electrode, is coupled with the quantum dot through a thicker insulator which does not allow noticeable tunnelling [3]. Therefore, electrons are injected into or ejected from the island through the tunnel junction. The number of electrons in the island can be controlled by using the gate electrode. Although a single-electron box can control the number of electrons in the island, it does not have the properties of a switching device which are essential elements of VLSI/ULSI circuits.
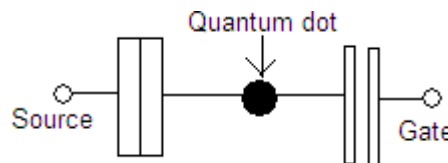

Fig. 2. Single Electron box

2.1   SINGLE ELECTRON TRANSISTOR (SET)

Single electron transistors are three-terminal switching devices. A schematic structure and equivalent circuit of an SET are shown in Fig. 3. The two tunnel junctions create a "Coulomb island or Quantum dot" that electrons can only enter by tunnelling through one of the tunnel junctions. The gate terminal is capacitively coupled to the node between the two tunnel junctions. The capacitor may seem like a third tunnel junction, but it is much thicker than the others so that no electrons can tunnel through it. The capacitor simply serves as a way of setting the electric charge on the coulomb island.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

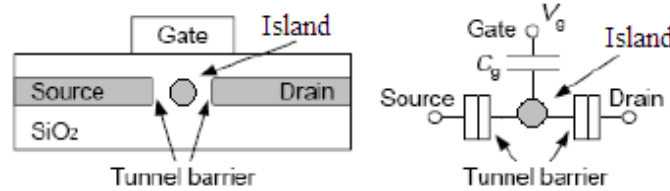## Vol. 2, Issue 12, DECEMBER 2013

Fig. 3. Schematic structure and equivalent circuit of SET

SET can transfer electrons form source to drain one by one and therefore can be used as a switching device. Electrons have to tunnel through the junction from the source to the drain via the central island for normal operation of the SET. For tunnelling to happen, the charging energy E_C should be greater than the thermal energy and also the tunnelling resistance R_T should be greater than the resistance quantum h/e^2. Therefore the conditions for observing single-electron phenomenon is expressed as $E_c = e^2/2C_\Sigma >> K_B T$ and $R_T >> h/e^2$ where C_Σ is the total island capacitance with respect to the ground, K_B is the Boltzmann's constant, T is the temperature and h is the Planck's constant. SETs may also have an optional 2nd gate connected to the island that can be used for controlling the phase shift of coulomb oscillation. The circuit schematic of such an SET is shown in Fig 4. In Fig 4, C_{TD} is the drain tunnel junction capacitance, C_{TS} is the source tunnel junction capacitance, R_D is the drain tunnel junction resistance, R_S is the source tunnel junction resistance, C_G is the gate capacitance and C_{G2} is the optional 2nd gate capacitance.
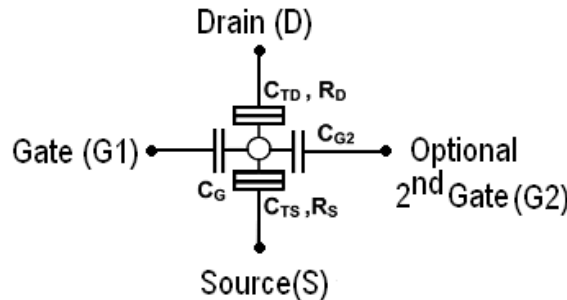

Fig. 4 Circuit schematic of SET with 2nd gate

2.2 MIB MODEL OF SET

The MIB model is a physically based compact analytical model for SET [5]. The model is based on the assumptions that it obeys the orthodox theory of single-electron tunnelling and the interconnect capacitances associated with the source, drain and gate are much larger than the device capacitance so that the total capacitance of the island with respect to ground will be equal to the summation of all device capacitances i.e $C_\Sigma = C_{TD} + C_{TS} + C_{G1} + C_{G2}$. Not all tunnelling current components are equally important and keeping only important tunnelling components of the current, the drain current in the MIB model for analog application is expressed as [5]

$$I_D = \lambda \frac{I_{TS}(0)I_{TD}(1) - i_{TS}(1)I_{TD}(0) + I_{TS}(1)\left(I_{TS}(0) + i_{TD}(0)\right) + I_{TD}(0)\left(i_{TS}(1) + I_{TD}(1)\right)}{(i_{TS}(1) + I_{TD}(1)) + (I_{TS}(0) + i_{TD}(0)) + I_{TS}(1)(I_{TS}(0) + i_{TD}(0))/I_{TD}(2) + I_{TD}(0)(i_{TS}(1) + I_{TD}(1))/I_{TS}(-1)} \quad (2)$$

where

$$I_{TS}(n) = \frac{\lambda V_{island} - (2n+1)\alpha}{\left[1 - \exp\left\{-\frac{\lambda V_{island} - (2n+1)\alpha}{V_T}\right\}\right] R_{TS}},$$

$$I_{TD}(n) = \frac{\lambda V_{DS} - \lambda V_{island} + (2n-1)\alpha}{\left[1 - \exp\left\{-\frac{\lambda V_{DS} - \lambda V_{island} + (2n-1)\alpha}{V_T}\right\}\right] R_{TD}},$$

$$i_{TS}(n) = \frac{-\lambda V_{island} + (2n-1)\alpha}{\left[1 - \exp\left\{-\frac{-\lambda V_{island} + (2n-1)\alpha}{V_T}\right\}\right] R_{TS}},$$

$$i_{TD}(n) = \frac{-\lambda V_{DS} + \lambda V_{island} - (2n+1)\alpha}{\left[1 - \exp\left\{-\frac{-\lambda V_{DS} + \lambda V_{island} - (2n+1)\alpha}{V_T}\right\}\right] R_{TD}},$$

n is the number of electron in the island, $\alpha = e/2C_\Sigma$ and λ holds the sign of V_{DS}.

Considering only '$0 \leftrightarrow 1$' transitions, the MIB model for digital application is expressed as [5]

$$I_D = \lambda \frac{I_{TS}(0)I_{TD}(1) - i_{TS}(1)I_{TD}(0)}{(i_{TS}(1) + I_{TD}(1)) + (I_{TS}(0) + i_{TD}(0))} \tag{3}$$

III. HYBRID SET-CMOS LOGIC GATES

The circuit of a Hybrid SET-CMOS Inverter proposed in Ref. 15, which is formed by a PMOS transistor as the load resistance of an SET is shown in Fig 5. Although it resembles a CMOS inverter, there are two differences [15]:

(a) The pull down transistor is an SET and
(b) V_{DD} is defined by the SET device parameters

Since the MIB model is valid for $|V_{DD}| \le 3e/C_\Sigma$ [7] for single/multiple gate(s) and symmetric or asymmetric SET devices, the bias voltage is taken as 800mV. The values of the tunnel junction capacitors (C_{TD} and C_{TS}) have been designed to prevent tunnelling due to thermal energy. The values of the parameters used for the devices are given in Table I.
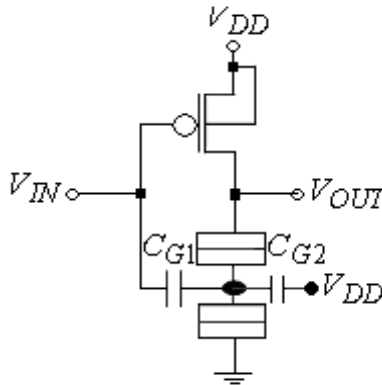

Fig. 5. Circuit of Hybrid SET-CMOS Inverter. V_{IN} is the input voltage and V_{OUT} is the output voltage.

Based on the idea that serial connection is AND and parallel connection is OR, the circuits of 2-input NAND, 3-input NAND and 4-input NOR are realized using the hybrid CMOS-SET inverter. The circuits of 2-input NAND, 3-input NAND and 4-input NOR are shown in Figs 6-8. The circuits of AND and OR can be realized by connecting an inverter at the output of NAND and NOR.

Fig. 6. 2-input Hybrid SET-CMOS NAND Gate: *A* and *B* are the input voltages and V_{out} is the output voltage.

Fig. 7. 3-input Hybrid SET-CMOS NAND Gate: *A, B* and *C* are the input voltages and V_{out} is the output voltage.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

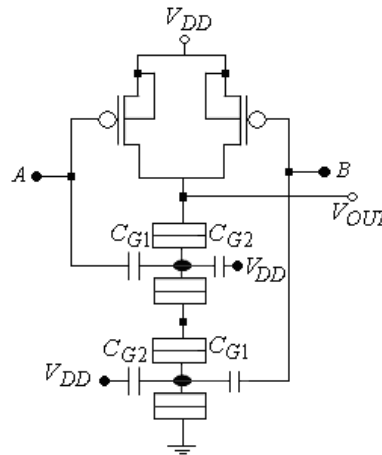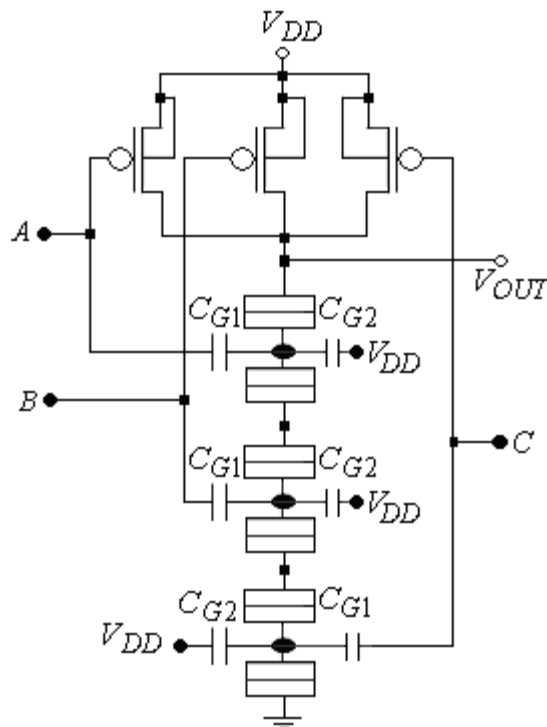*(An ISO 3297: 2007 Certified Organization)*
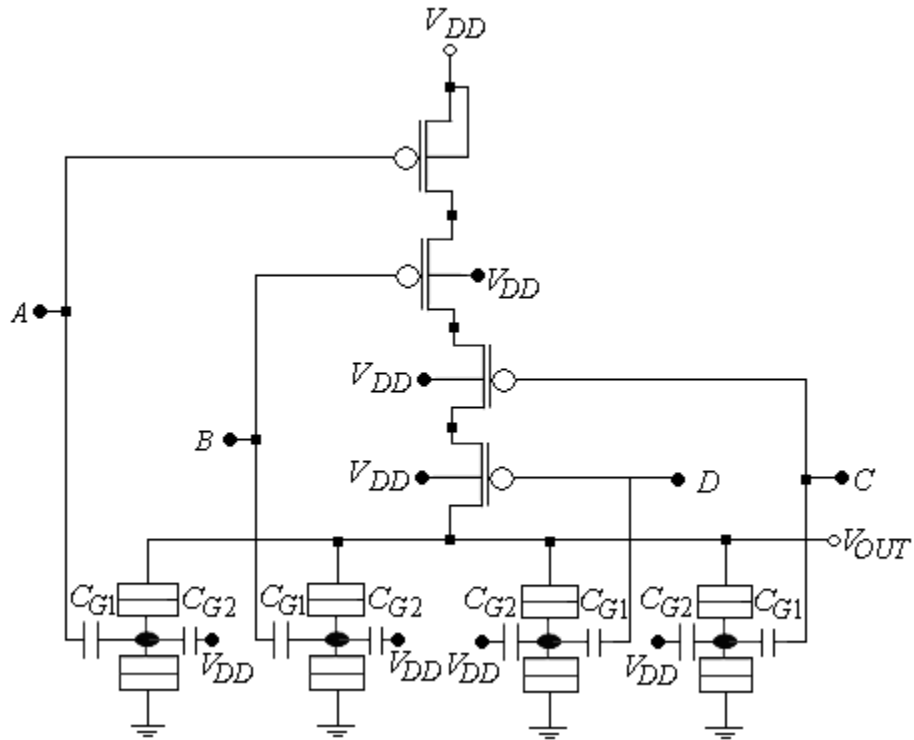
Vol. 2, Issue 12, DECEMBER 2013

Fig. 8. 4-input Hybrid SET-CMOS NOR Gate: *A, B, C* and *D* are the input voltages and V_{out} is the output voltage.

IV. DESIGN OF HYBRID SET-CMOS 4-TO-1 MUX AND 2-TO-4 DECODER CIRCUITS

The logic circuits for 4-to-1 MUX and 2-to-4 Decoder are shown in Figures 9 and 10. The design is done following conventional digital system design scheme and hence not detailed here. Using the structure of their CMOS counterparts, the circuits of 4-to-1 MUX and 2-to-4 Decoder implemented using the hybrid SET-CMOS logic gates are shown in Figures 11 and 12, respectively.

Fig. 9. Logic diagram of 4-to-1 MUX: A, B,C and D are the inputs, C_0 and C_1 are the control signals and Y is the output.

Fig. 10. Logic diagram of 2-to-4 DECODER. X and Y are the inputs, D_0, D_1 , D_2 and D_3 are the outputs

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

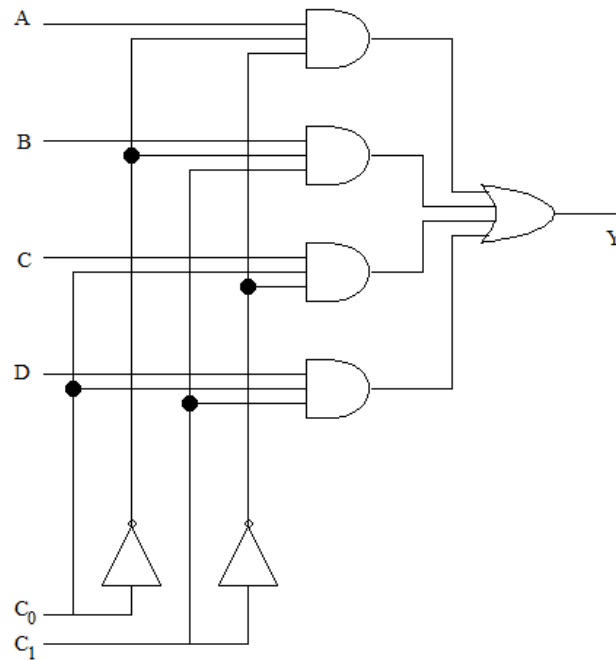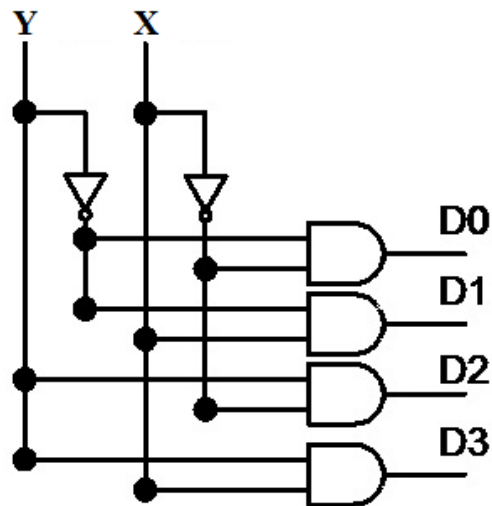*(An ISO 3297: 2007 Certified Organization)*
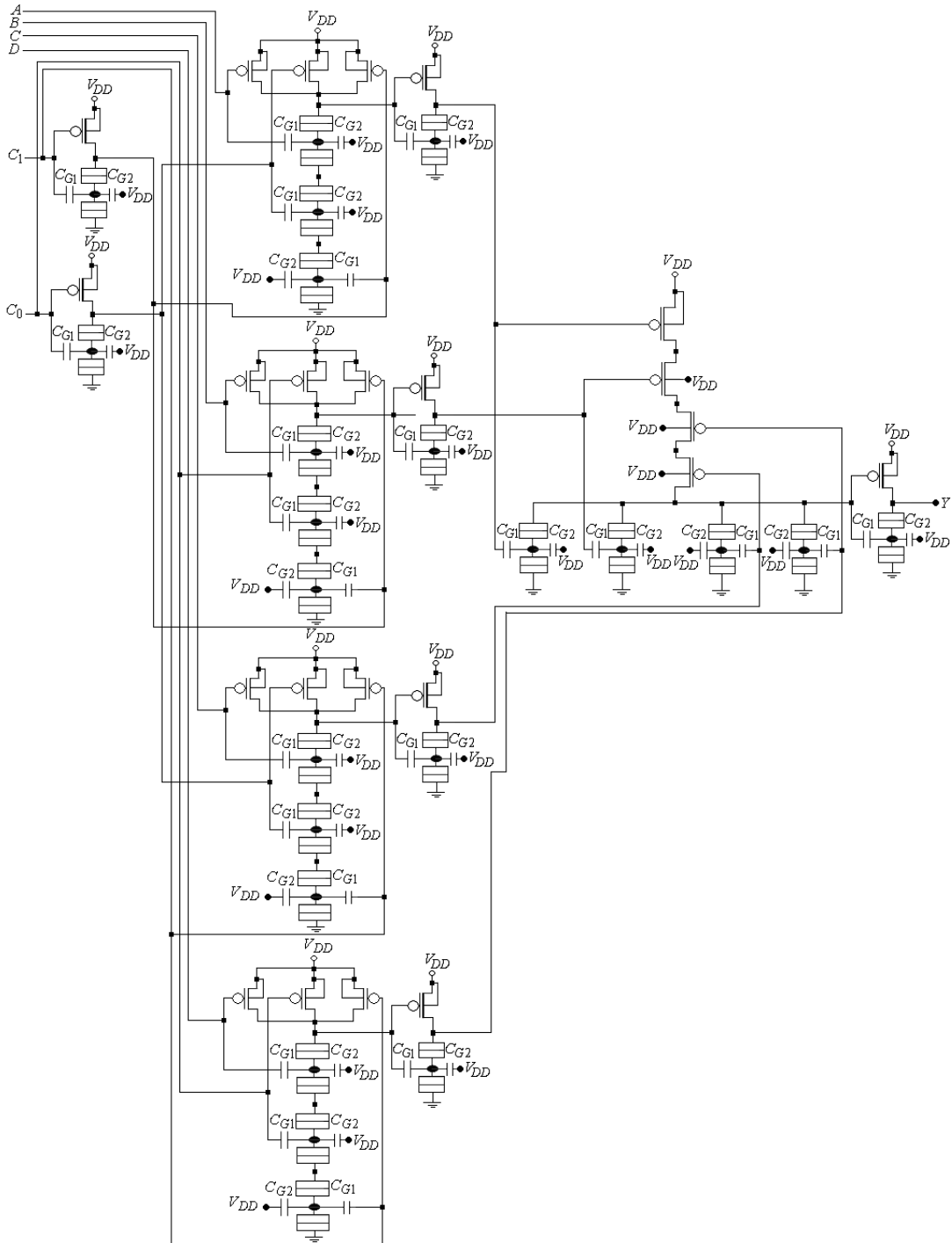
Vol. 2, Issue 12, DECEMBER 2013

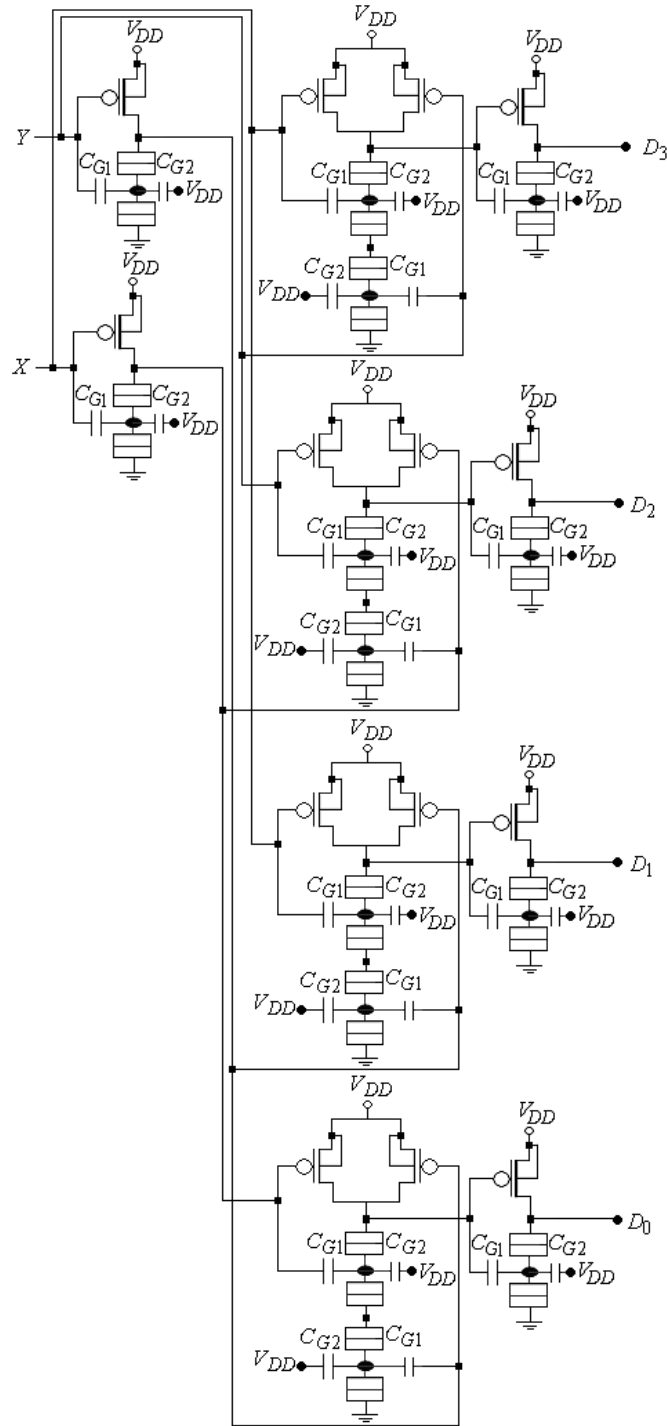
Fig. 11. Hybrid SET-CMOS 4-to-1 MUX. *A, B,C* and *D* are the inputs, C_0 and C_1 are the control signals and *Y* is the output.

Fig. 12. Hybrid SET-CMOS 2-to-4 DECODER. *X* and *Y* are the inputs, D_0, D_1, D_2 and D_3 are the outputs.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

V. RESULTS AND DISCUSSION

The proposed circuits are simulated using the MIB compact model described by Analog Hardware Description Language (AHDL) for SET and BSIM4.6.1 model for MOSFET in Tanner environment. The values of the parameters used for our simulation are given in Table I. The simulation result of Hybrid SET-CMOS 4-to-1 MUX is shown in Fig 13. A, B, C and D are the inputs, C_0 and C_1 are the control signals and Y is the output. The simulation result of Hybrid SET-CMOS 2-to-4 Decoder is shown in Fig 14. *X* and *Y* are the inputs, D_0, D_1 , D_2 and D_3 are the outputs. From Figs 13 and 14, it can be easily verified that the performances of Hybrid 4-to-1 MUX and 2-to-4 Decoder are satisfactory.

TABLE I
VALUES OF PARAMETERS USED FOR THE SIMULATION

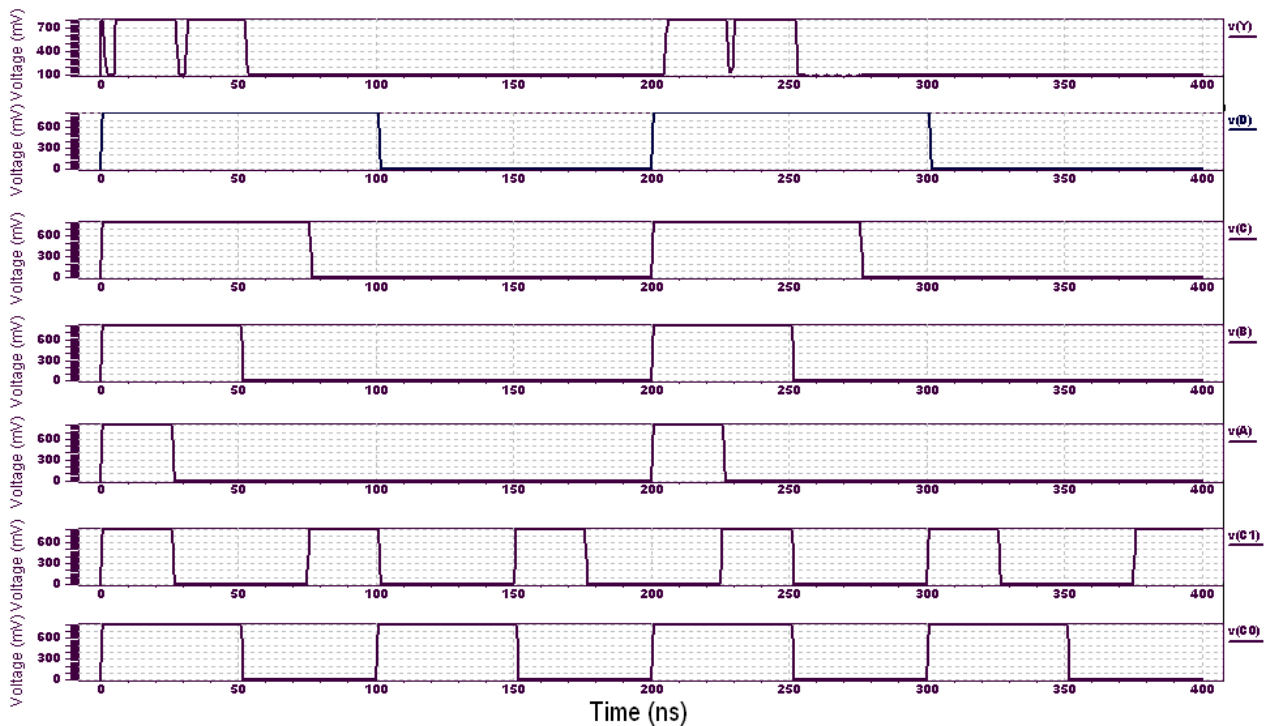| Device	Parameters	Voltage Level
SET	$R_{TD} = R_{TS} = 1M\Omega$, $C_{TD} = C_{TS} = 0.1aF$, $C_{G1} = 0.27aF$, $C_{G2} = 0.125aF$	Logic 0 = 0V Logic 1= 0.8V V_{DD}=0.8V
PMOS	$V_{TH} = -220mV$, W/L = 100nm/65nm and default values of BSIM4.6.1 model for other parameters	

Fig. 13. Simulation results for Hybrid SET-CMOS 4-to-1 MUX. A, B, C and D are the inputs, C_0 and C_1 are the control signals and Y is the output
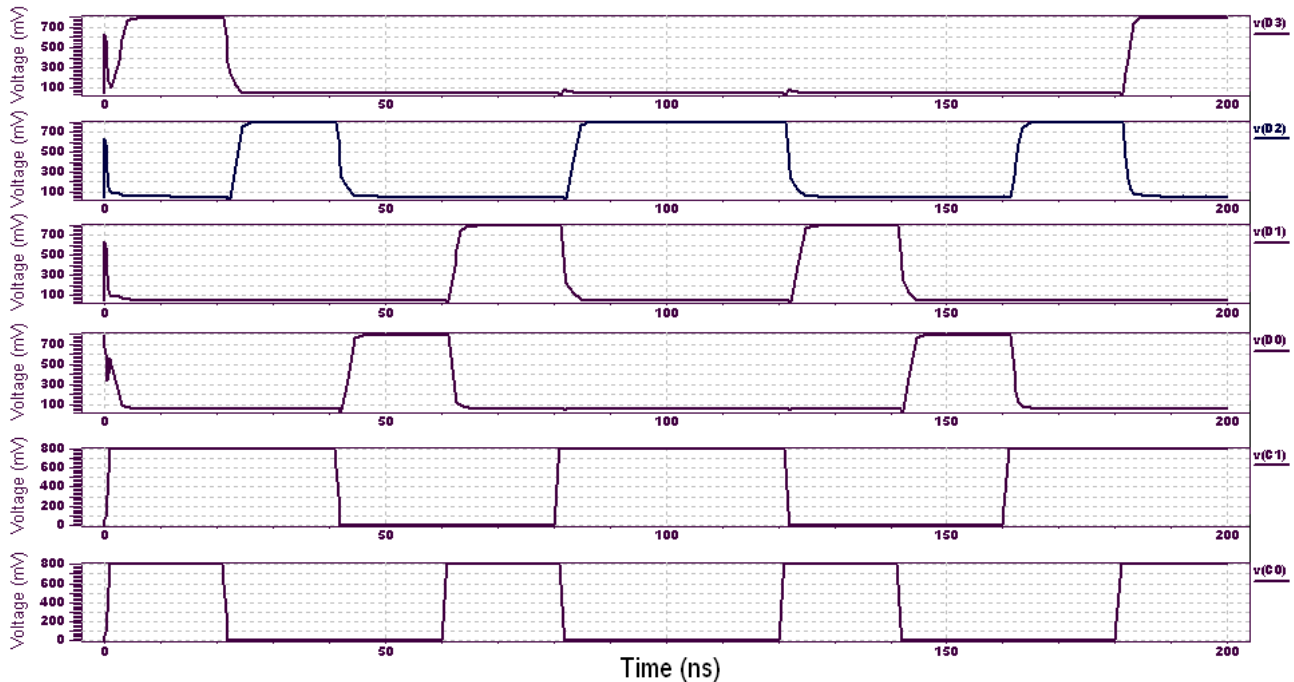
Fig. 14. Simulation results for Hybrid SET-CMOS 2-to-4 Decoder. . *X* and *Y* are the inputs, D_0, D_1 , D_2 and D_3 are the outputs

VI. CONCLUSION

The design and simulation of hybrid SET-CMOS 4-to-1 MUX and 2-to-4 Decoder are presented. The performances of the proposed circuits are verified by simulation using T-Spice simulation software. The simulation results show that the performances of the circuits presented in this paper are satisfactory thereby establishing the feasibility of using the proposed hybrid circuits in future low power ultra-dense VLSI/ULSI circuits.

REFERENCES

[1]   Christoper Wasshuber, "Computational Single Electronics", Springer Verlog Wien New York, 2001
[2]   T.A Fulton and G.J Dolan, "Observation of single electron charging effects in small tunnel junctions", Phys. Rev. Lett. Vol. 59, pp.109-112, 1987.
[3]   K Likharev, "Single-Electron Devices and Their Applications", Proc. IEEE, vol. 87, pp. 606-632, 1999.
[4]   M. Y. A. Ismail and R. A. Abdel Rassoul, "A New Simple Model for the single-Electron Transistor (SET)", IEEE, The 2006 International Conference on MEMS, NANO and Smart Systems, pp.7-10, 2006.
[5]   Santanu Mahapatra, Adrian Mihai Ionescu, " Hybrid CMOS Single-Electron-Transistor Device and Circuit Design" Artech House, Inc., 2006
[6]   Wancheng Zhang, Nan-Jian Wu, Tamotsu Hashizume, "Novel Hybrid Voltage Controlled Ring Oscillators Using Single Electron and MOS Transistors," IEEE Trans. on Nanotechnology, Vol. 6(2), pp 170-175, 2007.
[7]   Kyu-Sul Park, Sang-Jin Kim, In-Bok Baek etal., "SOI Single-Electron Transistor With Low RC Delay for Logic Cells and SET/FET Hybrid ICs" .IEEE, Trans. on Nanotechnology, Vol. 4(2), pp242-248, 2005.
[8]   S.Mahappatra, Adrian Mihai Ionescu, "Realization of Multiple Valued Logic and Memory by Hybrid SETMOS Architecture", IEEE, Trans. on Nanotechnology,Vol. 4(6), pp705-714, 2005.
[9]   H. Inokawa, A. Fujiwara, and Y.Takahashi,"A multiple-valued logic and memory with combined single-electron and metal-oxide-semi-conductor transistors," IEEE Trans. Electron Devices, vol. 50, no. 2, pp. 462–470, 2003.
[10]   S. Cotofana, C. Lageweg, and S. Vassilidis, "Addition Related Arithmetic Operations via Controlled Transport of Charge," IEEE Trans. On Computers, vol. 54, no.3, pp. 243-256, 2005.
[11]   D. V. Averin, and K. Likharev, "Coulomb blockade of tunneling, and coherent oscillations in small tunnel junctions," J. Low Temp. Phys. 62, 345-372, 1986.
[12]   C. Wasshuber, H. Kosina, "Recent advances and future prospects in single-electronics," Proc. of 2003 IEEE/ACM Design Automation Conference (DAC), pp. 274-275.
[13]   C. Lageweg, S. Cotofana, and S. Vassilidis, "Single Electron Encoded Latches and Flip-Flops," IEEE Trans. On Nanotechnology, vol. 3, no.2 (2004).
[14]   Jialin Mi; Chunhong Chen; "Finite state machine implementation with single- electron tunneling technology" IEEE Computer Society annual symposium on Emerging VLSI Technologies and Architectures, 2006.

[15]   A. Jana, N. Basanta Singh, J.K. Sing and Subir Kumar Sarkar, "Design and simulation of hybrid CMOS–SET circuits", 53, 4, 592–599, 2013.

BIOGRAPHY

Dr. N. Basanta Singh was born in Imphal, Manipur, India. He received the B-Tech degree in Electronics and Communication Engineering from Kerala University, Kerala, India in 1992, the M.E degree in Electronics and Communication Engineering from Thapar Institute of Engineering and Technology, Patiala, India in 2000 and the Ph.D Degree in Electronics and Communication Engineering from National Institute of Technology, Durgapur in 2013. He is currently Associate Professor and Head, Department of Electronics and Communication Engineering, Manipur Institute of Technology, Manipur University, Manipur, India. His current research interests include carrier transport in low-dimensional structures, modeling and simulation of nano-devices, SOI and SON MOSFETS, application of soft computing tools for parameter optimization of nanodevices and design and modeling of single electron devices.