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DESIGN AND ANALYSIS OF LOW POWER COMPRESSORS

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ABSTRACT: **The power management has become a great concern due to the increased usage of multimedia devices. Multipliers are the main sources of power consumption in these devices. The 3-2, 4-2 and 5-2 compressors are the basic components in many applications like partial product summation in multipliers. In this paper, various types of compressors have been designed. Different logic styles of XOR-XNOR gates and multiplexers have been compared with the existing CMOS logic. The pass transistor implementation of XOR-XNOR gates and multiplexer circuits achieves low power with less number of transistor counts. The proposed compressor architecture can be built using various combinations of XOR-XNOR gates, transistor level implementation and multiplexer circuits. The performance of basic compressor architectures with these low power XOR-XNOR gates and MUX blocks is found to be efficient in terms of area and power. Hence, the proposed 8x8-bit Wallace tree multiplier was designed using this proposed compressors and the power results are compared with the conventional Wallace tree multiplier design. The proposed Wallace tree multiplier using these compressors achieves significant amount of less power than conventional Wallace tree multiplier. The designs are implemented and power results are obtained using TANNER EDA 12.0 v tool.**

Keywords: Compressor, Multipliers, XOR-XNOR, Wallace Tree Multiplier.

I. INTRODUCTION

With the recent trends in increasing mobility and performance in small hand-held mobile communication and portable devices, among three thrust areas i.e speed, area and power, speed has become one of the significance in modern VLSI design. Parallel multipliers are used to speed up the processors compared to serial multipliers [1].

There are two basic approaches to enhance the speed of parallel multipliers, one of which is the Booth algorithm and the other is the Wallace tree compressors or counters [2].

Multiplier architecture can be divided into three stages, (1) partial product generation stage,(2) partial product addition stage and(3) final addition stage. Multipliers require high amount of power and delay during the partial products addition. For higher order multiplications, more number of adders or compressors are used to perform the partial product addition [3][4]. The numbers of adders were minimized by introducing different high order compressors.

Compressors logic based upon the concept of the counter of full adder. Compressors can be defined as single bit adder circuit that has four/five/six/seven inputs and three outputs [5]. Compressors form the essential requirement of high speed multipliers. The efficiency of the compressors is directly proportional the speed, area and power consumption of the multipliers.[6][7]

In this paper the compressor is designed using various XOR-XNOR, 2:1 Multiplexer and Transistor level implementation architecture. By using these designs, the power and delay are analyzed and the Wallace tree multiplier is designed using the high performance circuit.

The paper is organized as follows: Section 1 is the introduction of the compressors. Multiplier description is given in Section 2. Wallace tree and existing method is discussed in Section 3. The architectures of the compressors are discussed in Section 4. Section 5 deals with results and discussions. Finally conclusion of the paper is given in Section 6.

II. MULTIPLIER

A basic multiplier consists of three parts (i) partial product generation (iii) partial product addition and (iii) final addition. A multiplier essentially consist of two operands, a multiplicand "Y" and a multiplier "X" and produces a product. In the first stage, the multiplicand and the multiplier are multiplied bit by bit to generate the partial products. The second stage is the important stage, where the most complicated in determining the speed of the overall multiplier to add these partial products to generate the Product "P".

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This paper focused on the optimization of this stage. This stage consists of the addition of all the partial products. In high- speed design, the Wallace tree construction method is usually used to add the partial products in a tree-like fashion in order to produce two rows of partial products that can be added in the last stage.

III. WALLACE TREE MULTIPLIER

A fast process for multiplication of two numbers was developed by Wallace. By using the Wallace method, a three step process is used for the multiplication of two numbers; the bit products are formed. The bit product matrix are reduced to a two row matrix, where sum of the row equal to the sum of bit products, and two resulting rows of the bit product are summed with a fast adder(compressor) to produce a final product. The fig 1. shows the basic Wallace tree multiplier structure.

In the Wallace Tree method, three single bit signals are passed to a one bit full adder which is called a three input Wallace Tree circuit, and the output signal (sum) is supplied to the next stage full adder of the same bit, and the carry output signal thereof is passed to the next stage full adder of the same no of bit, and the carry output signal thereof is supplied to the next stage of the full adder located at a one bit higher position.

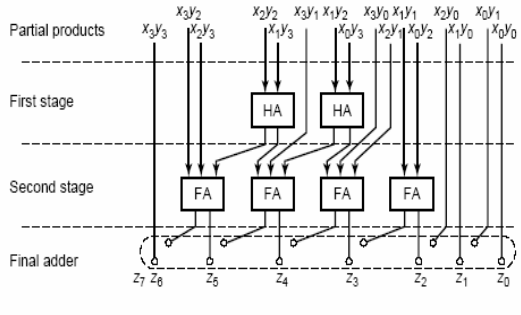

Fig.1. Wallace tree multiplier

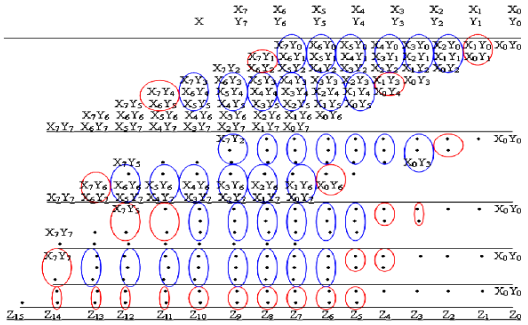

Fig.2.Conventional 8x8 bit Wallace Tree Multiplier

The above fig.2.shows the 14 T full adders is used for the existing design of the Wallace tree multiplier. By using this full adder circuit, the power consumption is high and the delay is increased during the partial product addition stage.

Compressor is mainly used to reduce the power consumption during the partial product addition stage and the critical path delay is also highly reduced.

IV. DIFFERENT TYPES OF COMPRESSOR ARCHITECTURE

V.

Different Compressor logic based upon the concept of counter of full adder. Compressor is defined as single bit adder circuit that has more than three inputs as in full adder and less number of outputs.

In the proposed architecture which is shown in Fig. 6, the fact that both the XOR and XNOR values are computed is efficiently used to reduce the delay by replacing the second XOR with a MUX. This is due to the possibility of the select bit at the MUX block before the inputs are applied. Thus the time taken for switching of the transistors in the critical path is highly reduced.

A 4:2 Compressor

The 4-2 compressor which has 4 inputs (x1, x2, x3 and x4) and 2 outputs (Sum & Carry) along with a Carry-in (Cin) and a Carry-out (Cout) as shown in Fig 3. The input Cin is the output from the neighboring lower significant compressor.

The Cout is the output to the next significant stage compressor.

It consists of two 3-2 compressors (full adders) in series and involves a critical path of 4 XOR delays which is shown in fig.4. An alternative implementation is shown in Fig.5. This implementation is better and involves a critical path delay of three XOR's, hence reducing the critical path by 1 XOR delay.

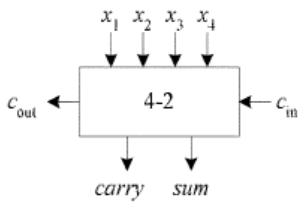

Fig.3. 4:2 Compressor

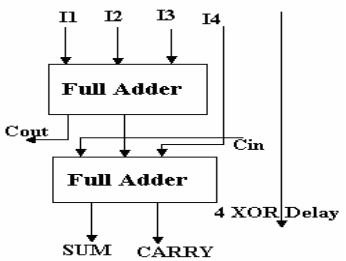

Fig.4. 4:2 Compressor using full adder

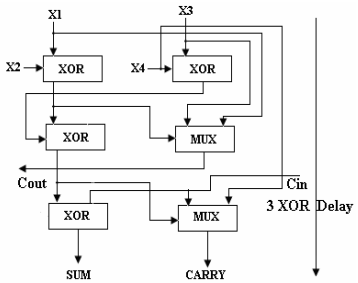

Fig.5. Alternative implementation of 4:2 compressor

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The output Cout, is independent of the input Cin accelerates the carry save summation of the partial products.

$$Sum = (x1 \oplus x2) \bullet \overline{x3 \oplus x4} + \overline{(x1 \oplus x2)} \bullet (x3 \oplus x4) \bullet \overline{Cin} + \overline{(x1 \oplus x2)} \bullet \overline{x3 \oplus x4} + \overline{(x1 \oplus x2)} \bullet (x3 \oplus x4) \bullet Cin$$
$$Cout = (x1 \oplus x2) \bullet x3 + \overline{(x1 \oplus x2)} \bullet x1$$
$$Carry = (x1 \oplus x2 \oplus x3 \oplus x4) \bullet Cin + \overline{(x1 \oplus x2 \oplus x3 \oplus x4)} \bullet x4 \quad (1)$$

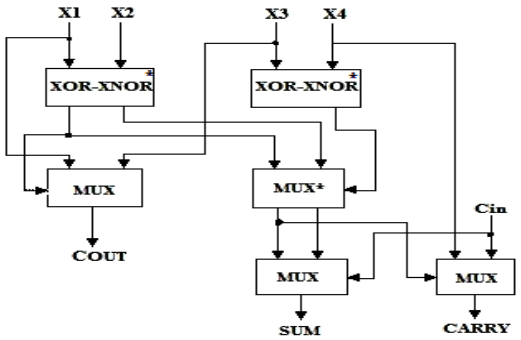

Fig.6. 4-2 Compressor using XOR-XNOR

B 5:2 Compressor

The 5-2 compressor is another widely used building block for high precision and high speed multipliers. The basic block diagram of a 5-2 compressor is shown in Fig. 7, which has seven inputs and four outputs. Five inputs are the primary inputs x1, x2, x3, x4 and x5, and the other two inputs cin1and cin2 receive their values from the neighboring compressor of one binary bit order lower in significance.

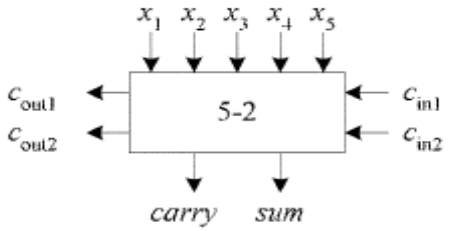

Fig.7. 5:2 compressor

In 5-2 compressor all of the seven inputs have the same weight. This compressor generates an output of the same weight as the inputs, and three outputs cout1, cout2, and weighted one bit binary higher order.
The output of the above basic 5:2 compressor is given below,

$$x_1 + x_2 + x_3 + x_4 + x_5 + c_{in1} + c_{in2} = \text{sum} + 2 \cdot (\text{carry} + c_{out1} + c_{out2}). \quad (2)$$

In the proposed architecture changes are to be made, to efficiently use the generated outputs at every stage. To obtain efficient output, few XOR blocks are replaced by XOR blocks with MUX blocks. In the proposed architecture these outputs are utilized efficiently by using multiplexers at select stages in the circuit. In this additional inverter stages are also eliminated. This contributes to the reduction of delay, power consumed and number of transistors.

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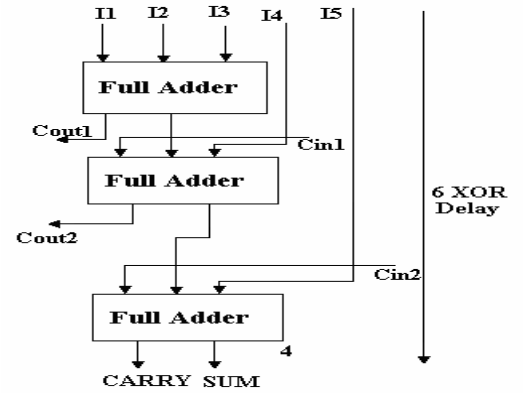


Fig.8. 5:2 Compressor using full adders

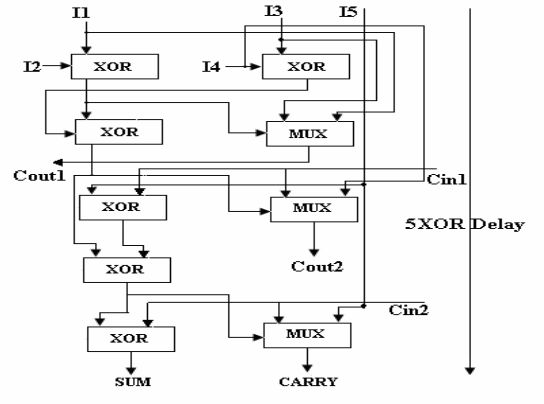


Fig.9. Alternative implementation of 5-2 compressor

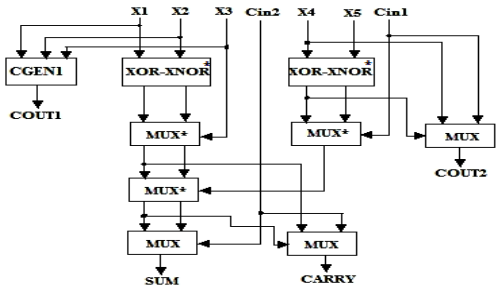


Fig.10. 5-2 Compressor block with XOR-XNOR

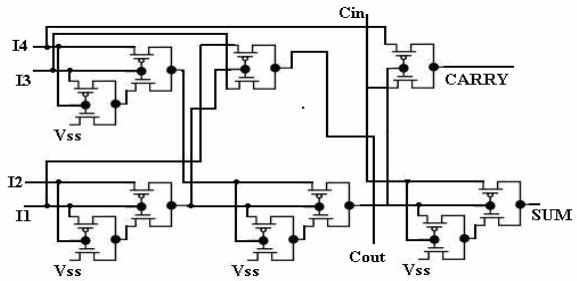
The above fig.10 shows the combination of XOR-XNOR which is used to design the 5-2 compressor.

C Transistor level implementation

1) 4:2 Compressor: The 4:2 compressor was initially designed by an intricate connection of two 3:2 compressor as shown in Fig.4. The structure has a delay of four XORs. The advantage of the structure lies in its free of carry, where the carry from the previous stage is not propagated to the next stage. A novel design of a 4:2 compressor with XORs and multiplexers (MUX) as building blocks is presented.

Then the 4:2 compressor is designed using XOR-XNOR circuit. By using this, the power consumption of the circuit is reduced and the delay is maximum reduced compared to the conventional compressor circuit.

The transistor level implementation is shown below. The optimal small area, low power and efficient throughput XOR design was proposed. The XOR design proposed in has no power supply and is referred as Powerless XOR. Thus, the 4-2 and 5-2 compressors are implemented with bare minimum of 20 and 30 transistors respectively.



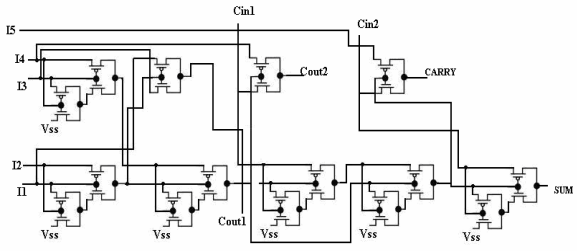


Fig.11. Transistor level implementation of 4-2 Compressor

Fig.12. Transistor level implementation of 5-2 compressor

VI. SIMULATION RESULTS

Logic gates in conventional or complementary CMOS are built from an NMOS pull-down and a dual PMOS pull-up logic network. In addition, pass gates or transmission gates are often used for implementing multiplexers, XOR-gates, and flip-flops efficiently. In this logic style, the XOR and XNOR outputs will be generated with the normal CMOS implementation with the transistor count of about 6 transistors in each unit, which is given in fig 13 and the output of the XOR-XNOR is shown in

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Fig 14.

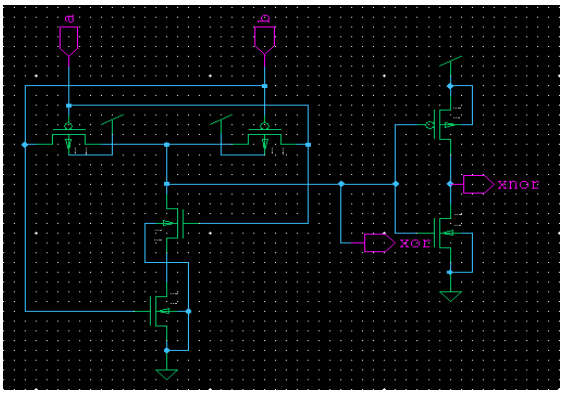

Fig.13. XOR-XNOR using 6 Transistors

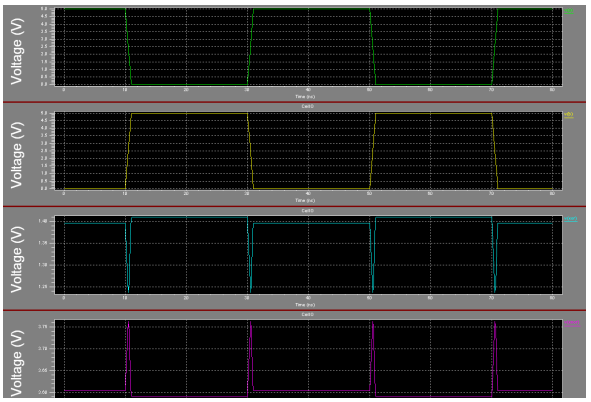

Fig.14. Simulation result of XOR-XNOR

The proposed 3-2 compressor architecture is given in fig 15. The 3-2 compressors using different XOR-XNOR gates and multiplexer circuits have been designed and power consumption is obtained for these compressor architectures.

The outputs functions of 3-2 compressors are given by

$$Sum = (x1 \oplus x2) \bullet \overline{x3} + \overline{(x1 \oplus x2)} \bullet x3$$

$$Carry = (x1 \oplus x2) \bullet x3 + \overline{(x1 \oplus x2)} \bullet x1 \quad (3)$$

The proposed 4-2 compressor is designed using XOR-XNOR gates and multiplexer blocks. The different XOR-XNOR styles with reduced number of transistor count have been used for analyzing power consumption. The 4-2 compressors using different XOR-XNOR gates and multiplexer circuits have been designed and power consumption is taken for these compressor architectures. The proposed 4-2 compressor architecture is given in fig 16.

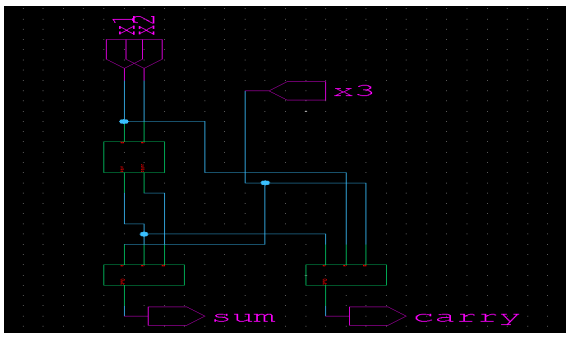

Fig.15. Proposed 3:2 compressor

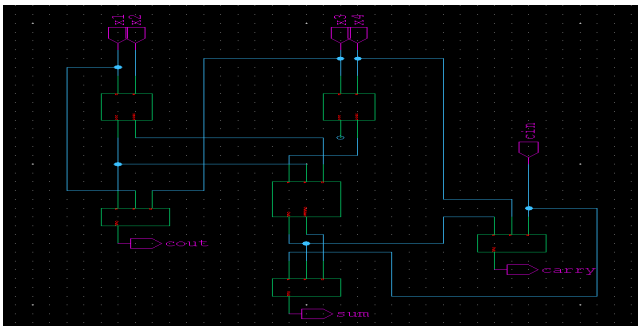

Fig.16. Proposed 4:2 Compressor

Transmission gate is basically used to avoid logic degradation. The nMOS passes logic low very efficiently but degrades high logic, where as pMOS passes logic high satisfactorily but degrades logic low. To overcome the above problems, transmission gates are used. Here the nMOS and pMOS both are connected together with their source and drain terminals.
Based on this logic a 2:1 Multiplexer is designed which is shown in fig 17. This design takes totally 6 transistors.

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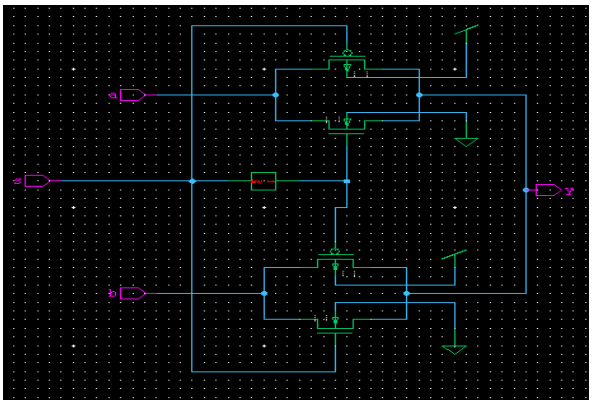

Fig.17. Transmission gate implementation of 2:1 MUX

A modified 8x8 multiplier architecture based on Wallace Tree, efficient in terms of power and regularity without significant increase in delay and area has been proposed. Here, the partial products are generated using AND gates. The modified Wallace tree is used for the addition of these partial products. The parallelism in generating the partial product is realized by ANDing the first bit (LSB) of the multiplier with the multiplicand bits. The second partial product is generated by ANDing the second multiplier bit with the multiplicand bits proceeded by a single zero. The third partial product is obtained by ANDing the third multiplier bit with the multiplicand bits preceded by double zeros.

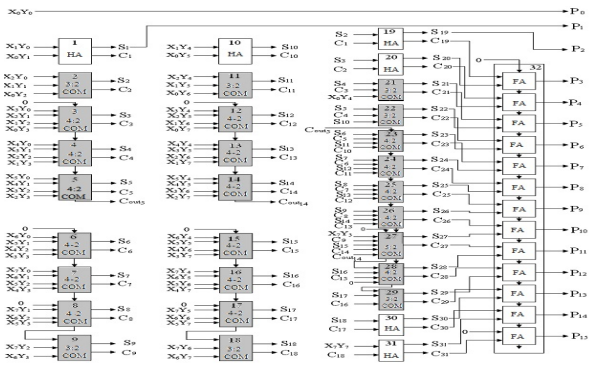

Fig.18. Proposed 8x8 Wallace Tre Multiplier using compressor

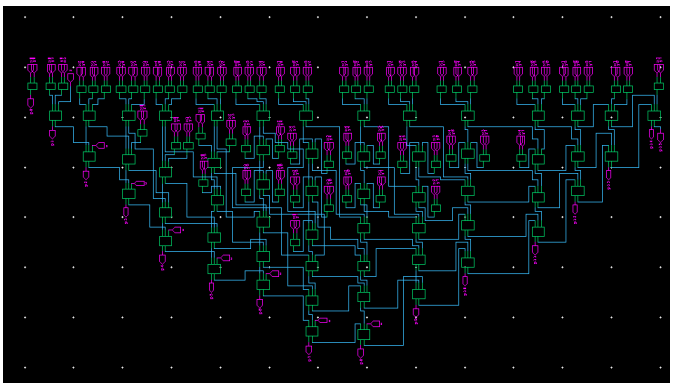

Fig.19. Schematic of 8x8 Wallace tree multiplier

Inputs (8-bit Multiplier And multiplicand)	Average power consumption in mW		Percentage %
	Conventional Wallace Tree (No of transistors:3774)	Proposed wallace Tree using compressors (1888)	
01100100 x 10001100	56.981	5.134	90.9
00111000 x 01100110	57.810	12.127	79
11100110 x 11001100	56.847	3.191	94.3
11000100 x 00111000	49.812	4.131	91.7

Table.1. Average power consumed for Wallace tree multiplier

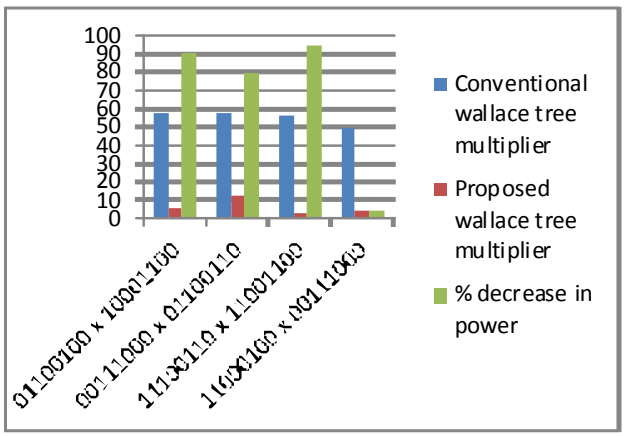

Fig.21. Power plot for table.1.

VII. CONCLUSION

This paper focused on the low power compressor which is used to design the Wallace tree multiplier. The conventional Wallace tree design 14 transistor adder cell is compared with the proposed 3-2, 4-2 and 5-2 compressor design with different logic styles. In proposed method the power consumption was highly reduced and the number of transistor count is also reduced. Due to this compressor, the area and speed of the Wallace tree multiplier is increased upto 24%. It was found that this is the efficient method for designing the Wallace tree multiplier.

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REFERENCES

[1] S. Veeramachanemi, K. Krishna, L. Avinash, S.R. Puppola,M.B. Srinivas, "Novel architectures for high-speed and low-power 3-2, 4-2 and 5-2 compressors," IEEE Proc. Oj VLSlD '07, pp. 324-329,2007.
[2] C. H. Chang, J. Gu, M. Zhang, "Ultra low-voltage low power CMOS 4-2 and 5-2 compressors for fast arithmetic circuits" IEEE Transactions on Circuits and Systems I:Regular Papers, Volume 51, Issue 10, Oct. 2004 Page(s):1985 – 1997.
[3] S. F. Hsiao, M. R. Jiang, and J. S. Yeh, "Design of high speed low-power 3-2 counter and 4-2 compressor for fast multipliers," *Electron. Lett, vol. 34, no. 4, pp. 341–343,*1998.
[4] H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10-transistor full adders using novel XOR–XNOR gates," *IEEE Trans. Circuits Syst. II, vol. 49, pp. 25–30, Jan. 2002.*
[5] R. Zimmermann and W.Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE J. Solid- State Circuits*, vol. 32, pp. 1079–1090, July 1997.
[6] Nabihah Ahmad, Rezaul Hasan, "A New Design of XOR-XNOR gates for low power application", IEEE conf,ICEDSA,2011.
[7] Hung Tien Bui, A.K. Al-Sheraidah, and Yuke Wang, "New 4-transistor XOR and XNOR designs," in Proceedings of the Second IEEE Asia Pacific Conference on ASICs, 2000, pp.25-28.
[8] Jyh-Ming Wang, Sung-Chuan Fang, and Wu-Shiung Feng, "New Efficient Designs for XOR and XNOR Functions on the Transistor Level," IEEE Journal of Solid-State Circuits, vol. 29, no. 7, pp.780-786, July 1994.
[9] Niichi Itoh, Yuka Naemura, Hiroshi Makino, Yasunobu Nakase, Tsutomu Yoshihara, and Yasutaka Horiba, "A 600-MHz 54 x 54-bit Multiplier with Rectangular-Styled Wallace Tree", JSSC,vol.36, no. 2, February 2001.
[10] K.Roy and S.C.Prasad, "Low power CMOS VLSI Circuit Design,"Wiley,2000.

BIOGRAPHY

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