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An Exhaustive Research Survey on Vedic ALU Design

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ABSTRACT: The digital India is playing an important role nowadays. Indian Vedas and Upanishads are also important and have a great history. That too Vedic mathematics was, is and will be an important basic logic for all mathematical related applications in various fields of science and technology. VLSI is an ever growing field which involves Analog, Digital and Mixed mode Designs. Also in VLSI research, an ALU is a very important system which involves user specifications while designing, for applications like microprocessor, microcontroller, signal processing and various fields. This paper concentrates on the related work on design of Vedic ALU, till date from 46 different IEEE papers and provides some common problem statements and solutions that can be used to design the best ALU, which is not done till date. Importance of reconfigurable feature is also explained in this paper.

KEYWORDS: Digital India, Vedas and Upanishads, Vedic ALU, Analog, Digital and Mixed mode Designs.

I. INTRODUCTION

Today's Digital computer systems are very important and built with several processor and controller units. In turn these processor and controller units do have heart, so called ALU (Arithmetic and Logic Unit). Nowadays, various constraints like low power consumption, lesser area and delay of various circuits and building blocks of processors are very important for a VLSI designer. In order to meet the constraints of VLSI Design to the satisfactory level, one has to optimize the processor and controller, which in turn is achieved by optimizing ALU using various techniques.

Veda means knowledge. "The Vedic mathematics", well known as the oldest mathematics, is a gift from our proud Indian ancestors. It includes sixteen different sutras and thirteen sub sutras (corollaries) that help for solving many simple to complex problems orally, mentally and practically. Today, Vedic mathematics is a boon for many researches in various domains just because of Jagadguru Shankaracharya Sri Bharati Krishna Tirthaji Maharaja of Govardhana Matha, Puri, who lived in between 1884 to 1960, and rediscovered the Vedic mathematics based on available Vedic manuscripts. It involves procedural steps to find a solution for various arithmetic and logical operations, in an easier and faster way.

In this paper, Section II explains the complete details of the related work carried out from 46 different IEEE papers over past four to five years. Then in section III, the actual problem statements and solutions that the real designers come across in designing a perfect ALU to meet various VLSI constraints are been summarized and this section is a very important part, as it is a sort of motivation for the research. Then in section IV, the actual conclusions of the entire survey and various research aspects on which VLSI designers can concentrate is discussed.

II. RELATED WORK

In paper [1], Arish S and R. K. Sharma, identified the problems in designing an area efficient multiplier. For the same, authors designed a multiplier using intellectual properties & optimized the design by truncating the inputs before performing the actual multiplication. Further using both Karatsuba and Urdhva Tiryakbhyam algorithm logic, authors were able to see the improvements in terms of area (Lesser Area). The authors also suggested that the optimization of model in terms of delay can be further done by using pipelining methods.

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In paper [2], Suryasnata Tripathy, et.al, proposed and presented a Vedic multiplier with 4 and 8 bits and using Urdhva Tiryakbhyam (UT) algorithm logic and the authors compared the same with the existing designs for various parameters like delay, area and power consumption using CMOS technology in Cadence EDA tool. Also the authors performed the performance analysis using several test inputs and concluded that their proposed designs were power efficient and operate at a high speed to provide the high performance results.

In paper [3], Savita Patil, et.al, proposed a high speed, low power multipliers using two different Vedic techniques i.e., Urdhva Tiryakbhyam and Nikhilam sutras of Vedic mathematics using 65nm CMOS Technology. The authors concluded that the improvement in terms of speed and power compared to the conventional array multipliers are obtained in that proposed designs.

In paper [4], Puneet Kachhwal and Bikash Chandra Rout, proposed and presented a square root algorithm using Vedic mathematic concepts and implemented on Spartan-3E FPGA kit and finally found that the design were less complex and operates at a higher frequency, occupies lesser area and need less power on comparison with the existing designs.

In paper [5], Vaijyanath kunchigi, et.al, proposed a square and cube architectures using Vedic mathematics. Finally the authors compared the designs with the existing conventional square and cube designs and found that the results were giving high efficiency, consuming lesser power, lesser area and operating at a higher speed.

In paper [6], Aravind E Vijayan, et.al, proposed an 8 bit Vedic multiplier architecture for image processing applications. The authors concluded that the proposed design requires lesser area and operates at very high speed compared to the existing architectures.

In paper [7], Abhyarthana Bisoyi, et.al, proposed a 32-bit Vedic multiplier and implemented the design on FPGA board and results were compared with the existing multipliers. Finally, the authors have concluded that the design operates at manageable speed but uses more LUTs and I/Os, and takes.

In paper [8], Premananda B.S., et.al, proposed an area and power efficient complex number multiplier using 8-bit Vedic mathematics. The authors implemented the designs in cadence encounter platform. Finally on comparison of proposed design with the existing ones, the results were concluded saying that the designs were consuming lesser area and were area efficient.

In paper [9], N. Rajasekhar and Dr. T. Shanmuganantham, proposed various compressors based adders, and modified the Vedic multiplier design and finally the authors concluded that the modified structure of Vedic multiplier was resulting with better speed and area performance.

In paper [10], Sitaramiah Venkataramana Srinivasan and Abdul Razak, proposed the chip for FFT application at the physical level in 90nm technology using Vedic mathematics and finally compared the same with the existing designs. The authors concluded that the proposed design consumed lesser area and operated at a higher speed compared to the existing ones.

In paper [11], Dalal Rutwik Kishor and V.S. Kanchana Bhaaskaran, proposed a low power, lesser gate requirement, low cost, and high speed divider using 45nm Technology in cadence, with the help of Vedic mathematics. The authors concluded that the proposed design was gives more efficient results in terms of gate count, power consumption and operating speed compared to the conventional divider circuits.

In paper [12], Surabhi Jain, et.al, proposed an optimized divider circuit that is used for various applications using Vedic mathematics techniques like Nikhilam and Parvartya sutras. The authors concluded that the proposed design shows much improvement in terms of lesser power consumption, lesser area and high speed operations compared to the conventional methods.

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In paper [13], Anjana.R, et.al, proposed a novel multiplier architecture that operates at a higher speed multiplication using Vedic mathematics. Apart from the basic block of multiplier circuit design, the authors even used the kogge stone adder. Finally the authors concluded that the combination of Vedic multiplier and kogge stone adder circuit resukts with the best multiplier and adder circuit compared to the conventional multiplier and adders.

In paper [14], Radheshyam Gupta, et.al, proposed a high performance 8 bit multiplier circuit using the combination of Vedic mathematics and various compressor circuits. The authors concluded that the results of the proposed Vedic compressor multiplier circuit resulted with more efficient performance, compared to the conventional types.

In paper [15], Sushma S. Mahakalkar and Sanjay L. Haridas, proposed a floating point multiplier IEEE754 standard circuit using Vedic mathematics and carry save adder combinations. The authors concluded that the combination of Vedic mathematics and carry save adder to design the floating point multiplier showed good performance in terms of area and speed, on comparison with the conventional types.

In paper [16], S. Hemalatha and V. Rajamani, focused on designing an efficient information security system for WSN applications using Vedic mathematic. The authors successfully designed the high performance VMIS (Vedic Mathematics Enabled information Security) compared to the conventional information Security for WSN Application. The authors concluded that the proposed design was successful because of Vedic mathematics.

In paper [17], Surabhi Jain and Sandeep Saini, presented a different kind of methods for DSP applications (convolution and deconvolution), by designing multiplier and divider circuit blocks using Vedic mathematics. The authors proved that the proposed design required lesser area and operated at higher speed on comparison with the actual convolution and deconvolution methods.

In paper [18], L. Sriraman, et.al, proposed a squarer using Vedic mathematics. The authors also compared the proposed design with the duplex squarer and concluded that the proposed design is best compared to the other in terms of speed of operation and power consumption.

In paper [19], Dani George and Bonifus PL, proposed a RSA encryption system with high performance. The authors concluded that the work was successful because of vedic mathematics, in terms of area, speed of operation and power consumption.

In paper [20], Yeshwant Deodhe, et.al, proposed an 8-bit Vedic multiplier using vedic mathematics concepts. Finally the authors concluded that the Vedic mathematics results with high performance in terms of area and power consumption on comparison with the conventional multipliers.

In paper [21], Ashwath M and Premananda B S, proposed a 32-bit Vedic multiplier using Urdhva Tiryakbhyam with carry save adder and ripple carry adder. Finally the authors concluded that the combination of vedic multiplier with carry save adder is better than the combination of Vedic multiplier with ripple carry adder in terms of speed by three times.

In paper [22], Arvind Kumar Mehta, et.al, proposed two different techniques; the first technique to convert the binary to BCD and other technique for N*N Vedic BCD multiplication. The authors suggested the Vedic mathematics logic can be used for the decimal arithmetic operations in future.

In paper [23], Sushma R. Huddar, et.al, proposed an 8-bit multiplier circuit using Vedic mathematics and compressors. The authors concluded that the proposed multiplier design occupied lesser area and operates at a faster rate compared to the existing multipliers.

In paper [24], Akhalesh K, et.al, proposed various DSP operations using Vedic mathematics concepts. Finally the authors compared the operating speed and area between proposed and conventional DSP operations and concluded that the proposed design is the best. The authors even suggested the Vedic logics can be further used for FFT and Filter applications also.

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In paper [25], P. Saha, D. Kumar, et.al, proposed a reciprocal unit using Vedic mathematics. The authors compared the proposed design with the Newton-Raphson's method to conclude that the proposed design was operating at a higher speed compared to the other.

In paper [26], Ratiranjan Senapati, et.al, proposed a novel binary divider for various VLSI applications using Vedic mathematics. The authors designed Vedic divider for the quotient part and suggested that the work can be further extended to remainder part calculation.

In paper [27], Mikhail Dorojevets and Nobuyuki Yoshikawa, proposed, tested and fabricated an ALU design that performs 8 arithmetic and 12 logical operations using wave-pipelining architecture. Finally the authors concluded that the area complexity is more and there were malfunctioning of certain operations.

In paper [28], Sushma R Huddar, et.al, proposed an area efficient and novel architecture for mix and inverse mix conversion operations, using Vedic mathematics for AES (Advanced Encryption Standard) applications. The authors concluded that the proposed designs were giving high performance in terms of area and speed of operation on comparison with two other conventional techniques.

In paper [29], Sandesh S. Saokar, et.al, proposed a multiplier block using Vedic mathematics, which is used for DSP application. Finally the authors concluded that the proposed DSP application using designed multiplier blocks operates at higher speed and suggested that the work can be further extended by using pipelining technique for maximizing throughput.

In paper [30], L. Sriraman and T. N. Prabakar, proposed a 16*16 multiplier circuit that uses Vedic mathematics and works at higher speed. The authors also concluded that the proposed multiplier gave higher performance for higher order bit multiplications.

In paper [31], Jubin Hazra, proposed a high speed low power DSP circular convolution application that operates at a higher speed and consumes lesser power using both Vedic mathematics sutras and Mutilple Channel CMOS (McCMOS) technique. The authors concluded that the hardware requirement is also very less. The authors also concluded that the power-delay product (PDP) of the proposed design on comparison with the conventional DSP circular convolution application was better.

In paper [32], Diganta Sengupta, et.al, proposed BCD division operator using Vedic mathematics. The authors concluded that the proposed model can divide numbers of up to 38 digits in a faster way, and also they concluded that the design required very less area and power and time to calculate the operation.

In paper [33], Prabir Saha, et.al, proposed a novel divider using Vedic mathematics. Finally the authors compared the proposed design with the conventional types and concluded that the proposed design results with high performance in terms of area and power consumption.

In paper [34], Prabir Saha, et.al, proposed a novel complex multiplier ASIC design using Vedic mathematics. The authors concluded that the design works at higher speed and can be used for various applications. Also the authors concluded that the proposed design showed improvements in terms of delay and power consumption.

In paper [35], Mr.R.G.Kaduskar, et.al, presented a Rivest-Shamir-Adleman (RSA) algorithm by using Vedic mathematics. The authors concluded that the proposed design is used in cryptography applications and yields the correct results.

In paper [36], Leonard Gibson Moses S and Thilagar M, proposed a RC6 algorithm for cryptography applications using Vedic mathematics. The authors concluded that the proposed design requires multipliers and the same could be designed using Vedic mathematics. Also the authors concluded that the performance and speed efficiency has been improved.

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In paper [37], Anvesh Kumar, et.al, proposed a reconfigurable FFT algorithm for DSP applications using Vedic mathematics. The authors concluded that the design provides the high performance and is flexible for carrying out some functional operations using very less power.

In paper [38], Anvesh kumar and Ashish raman, tried to propose a complete ALU design. But the authors are successful in designing only a part of ALU i.e., Multipliers using vedic mathematics. Further the proposed design was used for designing MAC unit and coprocessors of actual ALU processor.

In paper [39], Ramalatha M, et.al, proposed a cubing circuit using Vedic mathematics concepts. The authors found that the proposed design used lesser power, lesser area and worked at higher speed. The authors suggested that the proposed design can be further used for cryptography applications.

In paper [40], M. Ramalatha, et.al, proposed a part of ALU design using Vedic multipliers. The authors used Vedic mathematics in designing multipliers and the proposed design is used to design MAC unit. Finally the unit along with Adder and Subtractors were integrated to design part of ALU.

In paper [41], Honey Durga Tiwari, et.al, proposed both multiplier and square architecture using Vedic mathematics. The authors implemented the design on FPGA and the results in terms of area requirement and delay of operation were found to be very less on comparison with the conventional types.

In paper [42], Shamim Akhter, proposed a novel multiplier using vedic mathematics. The authors used the proposed basic multiplier for designing a N*N Vedic multiplier. The authors concluded that the design works at higher speed and requires lesser area and power.

In paper [43], S.Kumaravel and Ramalatha Marimuthu, proposed various vedic multipliers using karatsuba and booth algorithm techniques. Finally the authors concluded that the proposed design works at higher speed and suggested that the proposed design can suit the RSA cryptography applications.

In paper [44], Hanumantharaju M.C, et.al, proposed an area efficient, FPGA that gives high Performance and throughput using vedic multipliers. The authors concluded that the proposed architecture required very lesser area and operated at high speed.

In paper [45], Gayatri Mehta, et.al, proposed a reconfigurable fabric models for maintain FPGAs. The authors concluded that the feature called reconfigurable is like a reprogrammable; that could be used for reducing area requirement.

In paper [46], Himanshu Thapliyal, et.al, proposed a combination of both square and cube architectures using Vedic mathematics. The authors concluded that the design works at a higher rate on comparison with the conventional existing square and cube architectures.

III. PROBLEM STATEMENTS, EXPLANATION AND SOLUTIONS IN ALU DESIGN FROM SURVEY

From this survey, many common observations are observed related to the problems pertaining to VLSI designers, during the various stages of ALU design. Some common problems as notified in this survey are as follows and the possible solutions to overcome are also suggested.

Problem 1: Power Consumption of an ALU
Explanation: Today's worldwide technologies are facing various problems in the usage of power due to "energy crises". Hence the same case with an ALU also.
Solution 1: The total power consumption of an ALU has to be reduced by taking proper measures starting from initial to the final stages of the design. Also by using proper logic styles at the circuit level itself, one can reduce the total power consumption of the circuit. Even by applying various layout techniques and physical design rules like floor

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planning, clock tree synthesis, placing and routing techniques in a proper manner, the total power consumption can be reduced.

Problem 2: High Speed operation of an ALU
Explanation: There is an increasing demand for very high speed very large scale integration (VHSVLSI) ALU.
Solution 2: The speed of an ALU processor depends mainly on the time required to compute any task completely and also depends on the functional blocks involved in the process. Hence in order to increase the speed of ALU, proper design of all blocks of ALU using proper techniques have to be done carefully.

Problem 3: Area optimization of an ALU design
Explanation: Among various VLSI constraints like area, power and delay, area is very important aspect just because that there is a huge requirement of portable electronic gadgets like mobile phones, laptops, tablets and so on.
Solution 3: It can be done by using less number of transistors and proper design techniques.

Problem 4: Performance of an ALU
Explanation: Various applications of ALU like Microprocessors, Microcontrollers, FIR filters, Digital Signal Processors etc., demand the high performance.
Solution 4: The performance of these applications mainly depends on the numbers of arithmetic operation units like multiplication, additions, etc., and logical operation units like AND gates, OR gates, etc., used in performing unit task in a specified time bound.

Problem 5: ALU Processor Design Technology
Explanation: The ALU processor is required to handle simple, complex and challenging processes.
Solution 5: Proper kind of design technology is to be used in the design of ALU.

Problem 6: Loading problem of ALU
Explanation: Load on the processor is increasing day by day and hence it is a serious issue for achieving the successful system operation in a specified time bound.
Solution 6: It can be overcome by assembling the number of processor cores on the single IC, i.e., co-processors can be used along with the main ALU processor.

IV. CONCLUSIONS

To conclude, the ALU design which meets more than the real time user requirements for various applications can be done by using Vedic Mathematics concepts. Along with these aspects, using reconfigurable feature; one can reduce the power consumption, area and delay of various processors, which in turn helps to increase the speed of operation, efficiency and performance of various processor applications. Many works are been done using Vedic mathematics concepts, to design various units of ALU like multiplier, divider, squarer, cube, etc., separately. But no work is done with the combination of all these in a single ALU. Also without the tradeoff issues and by using reconfigurable feature, as well as proper solutions for all six problems as stated in section III, the best ALU can be designed that has combination of all arithmetic and logical operations using Vedic mathematics concepts, which is not done till date.

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