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A Resistorless CMOS Non-Bandgap Voltage Reference

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ABSTRACT: A resistorless CMOS nonbandgap voltage reference, which is compatible with 180nm CMOS Technology is presented in this paper. In order to reduce the temperature nonlinearity in proposed voltage reference, threshold voltage and a proportional to absolutely temperature (PTAT) voltage form the basic linear temperature components, which are achieved by resistorless threshold voltage extractor and differential difference amplifier. Besides, a self-biased current source is used to provide stable bias currents for the whole voltage reference, which can improve the power-supply noise attenuation (PSNA). Verification results of the proposed voltage reference simulated with 180nm CMOS technology demonstrate that the temperature coefficient (TC) of 10.5ppm/C with a temperature range of -20C to 80C is obtained at 1.8V power supply, and a PSNA of 86.2dB is achieved without any filtering capacitor while dissipating a maximum supply current of 22mA. The active area is 48.685mm47.645mm.

KEYWORDS: Resistorless, nonbandgap voltage reference, power supply noise attenuation, self-biased current source

I.INTRODUCTION

A voltage reference is a circuit that provides constant voltage irrespective of temperature or supply voltage variations. Voltage references are essential components in many electronic systems, such as data converters, power converters, dynamic random access memories, and radio frequency circuits. Low temperature and power supply sensitivity without modification of the fabrication process are critical requirements of a high-precision voltage reference. Besides, low power consumption requirement is one of the important design criteria in all systems.

The demand for low-power voltage reference with high precision is increasing. A voltage (or current) which is proportional to absolute temperature (PTAT) will be added to another voltage (or current) that is complementary to absolute temperature (CTAT) to obtain a reference voltage independent of temperature. A number of bandgap and non-bandgap voltage references designs have been implemented so far. It is very hard to find which design is the best.

Due to the nonlinear temperature characteristics of VEB, high-precision output voltage cannot be achieved without high-order temperature compensation approaches in conventional bandgap voltage references [1]. CMOS Voltage References Based on Threshold Voltage Difference are high precision voltage references based on weighted function of threshold voltages [2] (Vtn and Vtp) or weighted difference between the VGS[3]. Either additional fabrication steps or nonlinear temperature terms, such as carrier mobility, are included in the reference circuits. The circuits may include resistors, which worsen the immunity to substrate noise coupling. Therefore, high precision and low cost cannot be obtained at the same time. Besides, these designs compensate temperature dependence of mobility only at reference temperature.BGR described in [4]can be fabricated in standard CMOS technology without resistors. The BGR here uses only transistors biased in saturation or cutoff. The transistors biased in saturation, for which accurate device models are usually available, simplifying the design process. Trimming may be required for high precision applications. The low power can be easily achieved with the transistors biased in subthreshold region. The designs achieve a complete cancellation of the effects of temperature dependence of carrier mobility for any temperature [5]-[7]. Also channel length modulation and body effect are compensated. But the design process may be complicated by the transistors in subthreshold region, where accurate device models are not usually available and can be greatly

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influenced by the variations of the process. A self-biased symmetrically-matched current voltage mirror(SM CVM) is used in the design [8], which provides excellent line regulation. The design is similar to that of a conventional type BGR with the ordinary current mirror circuit is replaced with an SM CVM circuit. Resistors are included in the design. A theory is developed, states that the mutual compensation of mobility and threshold voltage may results in zero temperature coefficient bias points (ZTC) of a MOS transistor [9]. When a CMOS technology shows the presence of ZTC point, then this approach may provide a new family of voltage reference circuits. A low temperature coefficient voltage reference circuit without including resistors is described in [10]. The circuit is fabricated in standard CMOS technology. Neither special devices nor subthreshold transistors are required.

Resistorless voltage reference circuits can be advantageous since the circuit will occupy lesser area in the die, when compared to that of CMOS voltage references including resistors. Moreover, the resistorless circuits will be immune to substrate noise coupling. With the help of complementation linear-temperature terms, a low power nonbandgap voltage reference without any resistor is presented in this paper. Threshold voltage and a PTAT voltage form the basic linear-temperature components, which are achieved by resistorless threshold voltage extractor and differential difference amplifier. Besides, a self-biased current source is used to provide stable bias currents for the whole voltage reference, which can improve the power-supply noise attenuation (PSNA).

II.PRINCIPLE OF PROPOSED VOLTAGE REFERENCE

The basic idea of a resistorless CMOS voltage reference is the mutual compensation of thermal voltage, VT, which is a PTAT voltage, and threshold voltage of MOSFET, which is having CTAT behaviour. The two linear temperature terms are utilized to realize a low-temperature-dependent voltage reference with a significant reduction of non-linear temperature terms. A self-biased current source is used to provide stable bias currents for whole voltage reference.

The Fig. 1 shows the main idea of the proposed voltage reference circuit. It includes a threshold voltage extractor (TVE), circuit to extract the thermal voltage using base emitter voltage difference, ΔVBE. A differential difference amplifier is used to combine the two non-linear temperature terms to generate a constant output voltage.

In order to avoid the influence of VBEs nonlinearity temperature characteristics, threshold voltage with linear temperature dependence is adopted in the proposed voltage reference. whose magnitude function is modeled as

$$|V_{TH}(T)| = |V_{TH}(T_0)| - \alpha V_T(T - T_0) \quad (1)$$

where T is absolute temperature, T_0 is the reference temperature, $V_{TH}(T_0)$ is the threshold voltage at temperature T_0, αV_T is the TC of the threshold voltage, which is usually a positive constant in conventional technologies. From the above equations, it is clear that the threshold voltage of an nMOS transistor have negative temperature coefficient. On average this value ranges from -4mV/K to -2mV/K depending on doping level. Several circuit designs are there to extract the threshold voltage of a MOS transistor. Choosing a simple design and incorporate it properly in the proposed design is the major issue.

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Fig. 1 Main idea of the proposed voltage reference

A PTAT voltage (thermal voltage, V_T) can easily be obtained by taking the difference of two base-emitter voltages of two transistors of different emitter area. In conventional BGR circuits, this is achieved with the help of resistors in the circuit. In the proposed design the idea of conventional BGR is used to obtain a PTAT voltage, except that the resistor in the circuits is replaced with a MOSFET operating in triode region. An equivalent current, which is the bias current for the entire circuit, which is also PTAT in nature can also be obtained.

$$V_{PTAT} = \Delta V_{BE} = V_T \ln(N) \quad (2)$$

where N is the emitter area ratio of the transistors used to obtain the voltage ΔVBE.

The self-biased current source can provide a stable bias current for the whole voltage reference. The circuit can also help the PTAT extractor to obtain its necessary biasing conditions. For simplicity and less overdrive a simple current mirror circuit can be used as current source. The self biasing also provides better line regulation for the voltage reference.

With the help of generated bias current in SBCS, a weighted PTAT term can be realized in DDA. Superimposing this PTAT term on threshold voltage extracted by TVE using the DDA, without additional circuit, a reference voltage can be obtained.

III.CIRCUIT OF PROPOSED VOLTAGE REFERENCE

The functions and design requirements of various circuit elements in the resistorless CMOS nonbandgap voltage reference circuit are discussed in the following sections.

A. PTAT GENERATION

PTAT term for the proposed ciruit is obtained from ΔVBE. The base emitter voltage of bipolar transistor is having CTAT nature.

$$V_{BE} = V_T \ln(I_0/I_S) \quad (3)$$

where I_0 is the constant current flowing through the bipolar transistors, I_S is the scale current or the reverse bias saturation current.

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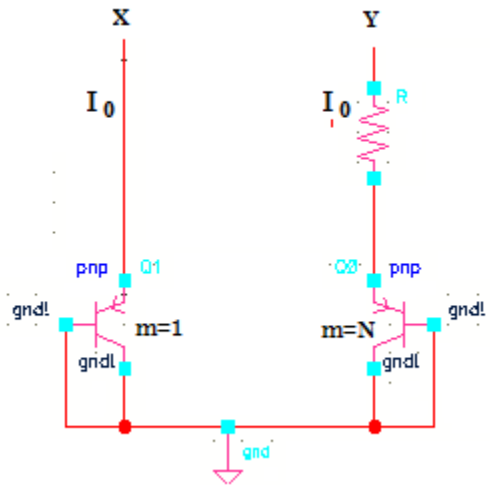

Figure 2: PTAT generation

Consider two branches with same current and same potential at points X and Y as shown in Fig. 2. Now the voltage across the resistor can be written as

$$V_r = \Delta V_{BE} = \frac{VT \ln(I0/IS)}{VT \ln(I0 / N\ IS)} = V_T \ln(N) \tag{4}$$

where V_T is the thermal voltage with value 26 mV/°C. Thus a PTAT voltage can be obtained. By replacing this resistor with an nmos operating in triode region having, a resistorless circuit can be obtained. The current through the transistor can be expressed as

$$I_{bias} = V_T \ln(N) / r_o \tag{5}$$

This is the bias current for whole of the circuit. The resistance r_o is the equivalent output resistance of the nMOS transistor used instead of the resistor.

B. ***SBCS***

The SBCS circuit comprised of a simple current mirror circuit with some arrangements to bias the circuit. The current mirror circuit will provide same current through the branches. The nMOS transistors N_{M1} and N_{M2} are biased such that they will be operated in saturation region. The gate voltages of NM_1 and NM_2 are equal, also the current through them are also equal. Thus, the source voltages will also be equal. Their sources will be assigned as points X and Y.

$$I_X = I_Y = I_0 \tag{6}$$
$$V_{G\_NM0} = V_{G\_NM1} \tag{7}$$
$$\therefore V_{S\_NM0} = V_{S\_NM1} \tag{8}$$

i.e., $V_X = V_Y$. Thus the requirement for PTAT generating circuit can be obtained.

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C. TVE

Required conditions for the threshold voltage extractor ciruit are

(1) All transistors except N_{M4} should be in saturation. Transistor NM_4 sholud be in triode region.
(2) The overdrive voltage of transistors NM_3 and NM_5 should be equal.

According to the Kirchhoff's theorem,

$$V_{GS\_NM4} = V_{GS\_NM5} + V_{DS\_NM4} \tag{9}$$

Based on the voltage-current relationship of MOSFETs in strong inversion region, the voltage difference between nodes A and B is equal to V_{OV}. The output voltage of proposed RLTVE, V_{PTTV}, can be expressed as

$$V_{PTTV} = V_{TH\_NM3} \tag{10}$$

where V_{TH_NM3} is the threshold voltage of NM_3. Therefore, V_{PTTV}, which is proportional to threshold voltage (PTTV), is successfully obtained without any resistor. V_{PTTV} has strong linear negative temperature behaviour without the nonlinear temperature influence of carrier mobility.

D. DDA

The DDA will take threshold voltage as one of the gate input. The second input gate voltage will be set as reference voltage, such that the resulting drain current in that transistor is a PTAT term which is proportional to the bias current, I_{bias}.

$$V_{diff} = V_{REF} - V_{PTTV} \tag{13}$$

$$\therefore V_{REF} = V_{diff} + V_{PTTV} \tag{14}$$

This input voltage difference V_{diff} is proportional to the current I_D. The output reference voltage V_{REF} can be represented as $V_{REF} = I_D$ gm, where gm is the transconductance of the transistor. The fig. 3 shows the circuit of the proposed voltage reference.

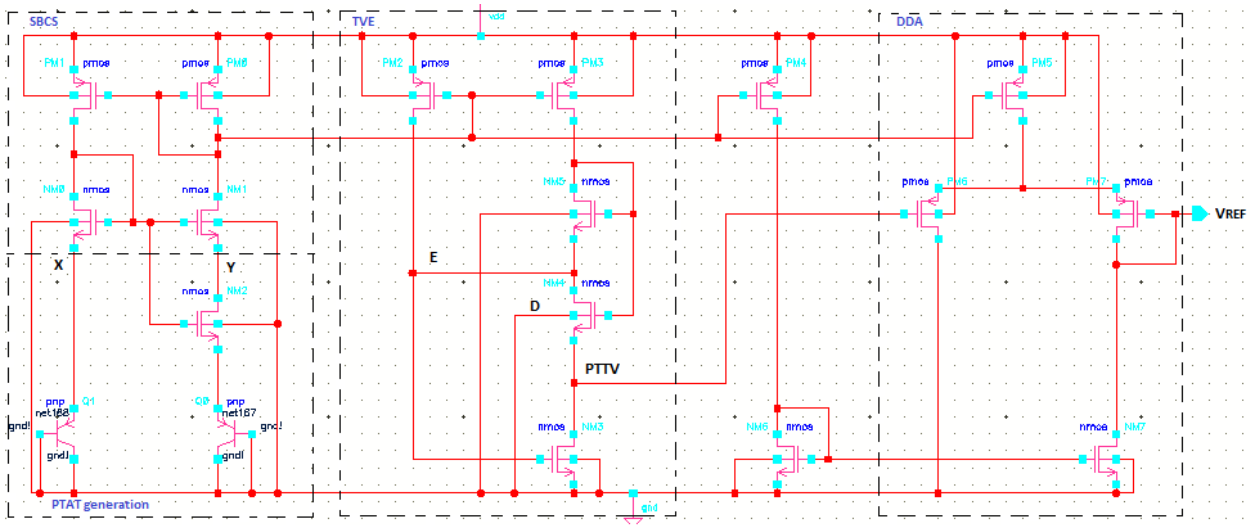

Fig. 3: Schematic of the resistorless voltage reference circuit

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IV. SIMULATION AND RESULTS

Fig. 4 is the plot of output reference voltage as a function of temperature. From the graph, the TC of the output reference voltage V_{REF} is in the range of 10.5ppm/◦C to 28ppm/◦C.

The Fig. 5 is the plot of line regulation. The graph is plot by varying the supply from 0V to 5V. From 1.75V the circuit will work properly. The line regulation is found to be 44mV/V.

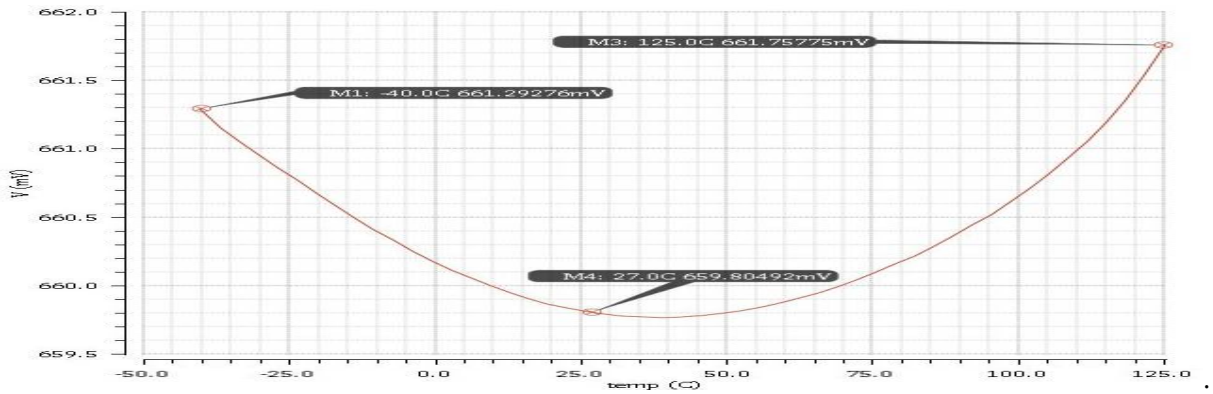

Fig. 4: V_{REF} Vs Temperature

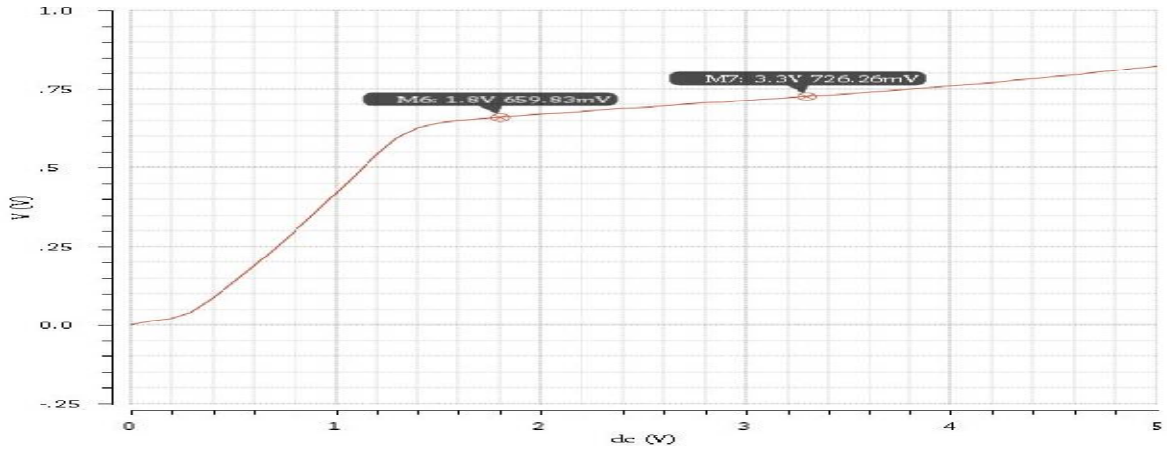

Fig.5: V_{REF} Vs V_{DD}

For the calculation of power supply rejection ratio, a noise voltage source will be added at the power supply rail. AC analysis is carried out by sweeping the frequency of noise source and monitoring the change in output reference voltage.

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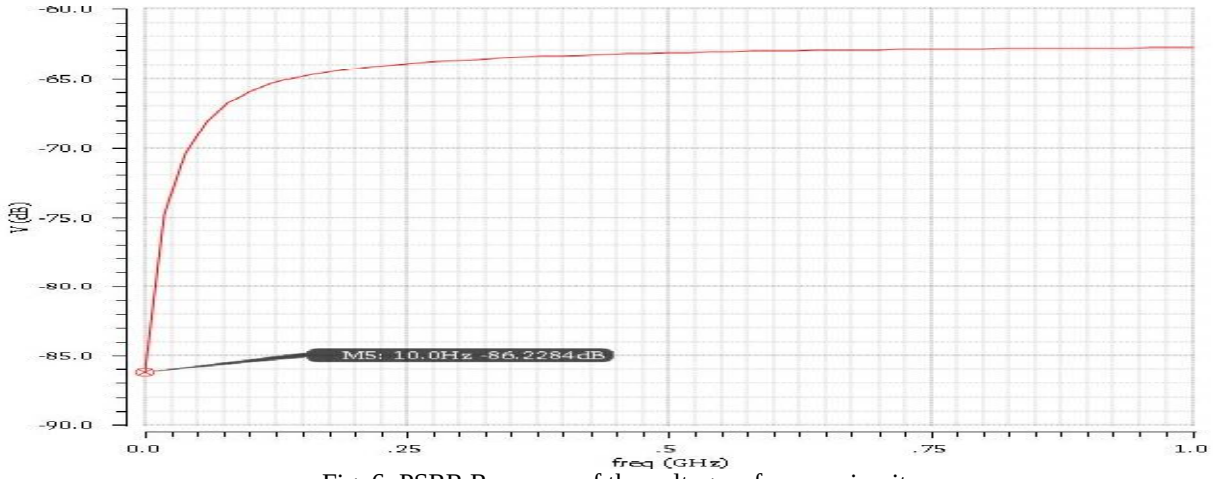

Fig. 6: PSRR Response of the voltage reference circuit

Power supply rejection ratio is calculated as the ability of the voltage reference circuit to reject the noise on the power rail and to provide a stable reference voltage. It is the ratio of output reference voltage to the input power supply noise voltage at a particular frequency. The power supply rejection ratio obtained by this circuit is around 86dB. The negative indicates that it is attenuation. So even if there is a voltage variation in the input power supply, it does not change the output reference voltage drastically.

Quiescent current is the current required to operate the voltage reference circuit at steady state condition with no resistive load. A voltage reference circuit with a low quiescent current is desirable for two reasons. First, it implies high power efficiency and long working hours, second, will have a small power dissipation and hence a small self-heating effect which helps to maintain accuracy and stability of the output voltage of the voltage reference circuit. The quiescent current for the designed voltage reference is around 22µA.

An ever-present challenge in electronic circuit design is selecting suitable components that not only perform their intended task but also consumes less power. For battery powered systems the power consumption is a critical factor, it should be kept low so that the entire system is having extended life. The power consumption of this resistorless voltage reference is around 40µW.

Layout of the proposed voltage reference is shown in Fig. 7. From the layout the chip area is found to be 48.685µm × 47.645µm.

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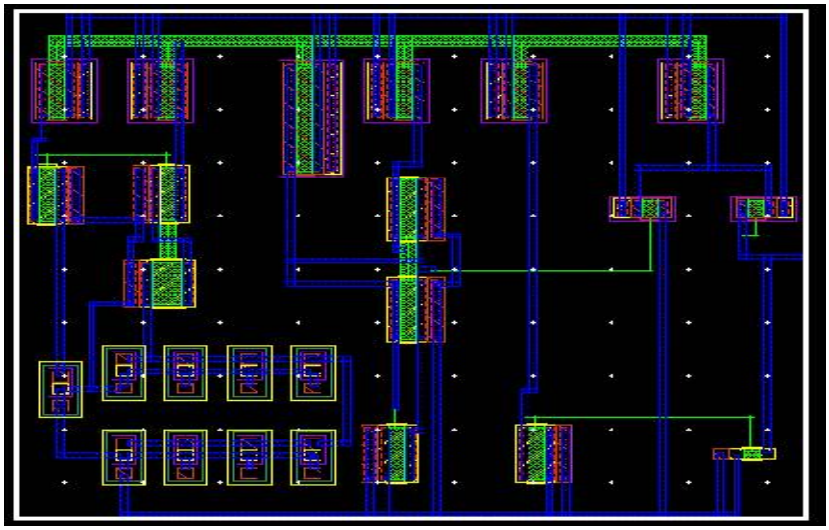

Fig. 7: Layout of the proposed voltage reference

V. CONCLUSIONS

A resistorless nonbandgap voltage reference has been designed and simulated by standard 0.18μm CMOS technology, based on the linear-temperature complementation of threshold voltage and PTAT voltage. A high-precision output with low power has been achieved. A TVE circuit is presented to obtain threshold voltage of transistors. Combined with an SBCS circuit and a DDA circuit, the output current of the DDA is made proportional to absolute temperature, and the superposition of the two linear-temperature terms is realized at the same time. Since no additional component is needed, the proposed voltage reference is completely compatible with digital CMOS technologies.

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