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A New Single Phase Single Stage Three Level Power Factor Correction Ac/Dc Converter

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ABSTRACT: AC-DC power electronic converters are widely used for electrical power conversion in many industrial applications such as for telecom equipment, information technology equipment, electric vehicles, space power systems and power systems based on renewable energy resources. Conventional AC-DC converters generally have two conversion stages, an AC-DC front-end stage that operates with some sort of power factor correction to ensure good power quality at the input, and a DC-DC conversion stage that takes the DC output of the front-end converter and converts it to the desired output DC voltage. Due to the cost of having two separate and independent converters, there has been considerable research on so-called single-stage converters. Converters that can simultaneously perform AC-DC and DC-DC conversion with only a single converter stage. Elimination of one of these stages reduces the cost, weight, size, complexity and increase the overall reliability of this converter. The main focus of this thesis is on development of new and improved AC-DC single-stage converter that is based on multilevel circuit structures (topologies) and principles instead of conventional two-level the drawbacks of previous proposed converters are reviewed. A variety of new power electronic converters including new single-phase and a new DC-DC converter are then proposed. A new three-level single-stage power factor- corrected AC-DC converter is presented. The proposed circuit integrates the operation of a boost power factor correction converter and a three-level DC/DC converter into one converter. The Proposed converter does not have the problem of high component stress due to high rising intermediate bus voltages that other single-stage converters have because of its three-level structure. It can operate over a wider load range with significantly less output inductor current ripple; moreover, its input current has little distortion. In the thesis, the operation of the new converter is explained in detail and analyzed, its steady-state characteristics are determined, and its design is discussed.

KEY WORDS: Power Factor Correction (PFC), AC–DC power conversion, single-stage power factor correction (SSPFC), Three level converters.

I. INTRODUCTION

The power supply unit is an essential circuit block in all electronic equipment. It is the interface between the ac mains and the rest of the functional circuits of the equipment. These functional circuits usually need power at one or more fixed dc voltage levels. Switch mode power supplies (SMPS) are most commonly used for powering electronic equipment since they provide an economical, efficient and high power density solution compared to linear regulators. The devices generally used in industrial, commercial and residential applications need to undergo rectification for their proper functioning and operation. They are connected to the grid comprising of non-linear loads and thus have non-linear input characteristics, which results in production of non-sinusoidal line current. Also, current comprising of frequency components at multiples

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of line frequency is observed which lead to line harmonics. Due to the increasing demand of these devices, the line current harmonics pose a major problem by degrading the power factor of the system thus affecting the performance of the devices. Hence there is a need to reduce the line current harmonics so as to improve the power factor of the system. This has led to designing of Power Factor Correction circuits. Power Factor Correction (PFC) involves two techniques, Active PFC and Passive PFC. Here active power factor circuit Converter was designed for improving the power factor. This converter is to observe the effect of the active power factor corrector on the power factor. The advantage of using power factor correction circuits is that to obtain better line regulation with appreciable power factor. Active PFC can be implemented by controlling the conduction time of the converter switches to force the ac current to follow the waveform of the applied ac voltage.Passive PFC is the simplest and most straightforward method to eliminate input current harmonics. This is achieved by using passive reactive elements either at the input or at the output side of input rectifier employed in the design of AC-DC converter. Advantages of this method are high efficiency, low EMI and simple implementation. However, the main drawbacks particularly at the low frequency are the size, weight and cost.

II. PROPOSED CONVERTER

Voltage-fed, single-stage power factor correction (SSPFC) full-bridge converters are attractive because they cost less than two-stage converters, but their use has been limited because of the drawbacks that they have. Most of these drawbacks are because they are controlled by a single controller that regulates the output voltage so that the dc bus voltage is left unregulated. As a result, the primary-side dc bus voltage of these converters may become excessive under high-input-line and low-output-load conditions. Measures can be taken to limit the dc bus voltage so that does not become excessive, but these measures affect the performance of voltage-fed, SSPFC full-bridge converters in several ways. The input power factor of a single-stage voltage-fed SSPFC converter is not as high as that of current-fed converters. The output inductor current of a single-stage voltage-fed SSPFC converter is discontinuous for all operation conditions, which results in higher secondary-side component peak current stresses. The performance of voltage-fed, SSPFC full-bridge converters can be improved if the limit on the dc bus voltage (typically < 450 V) is relaxed. This is not something that can be done for SSPFC full-bridge converters that are based on two-level topologies, but this can be done for converters that are based on three-level, multilevel topologies as the primary-side switching devices of these converters are exposed to half the peak voltage stress that those of two-level converters are. As a result, the dc bus voltage limit can be doubled for multilevel converters, but the peak voltage stress of the switches is the same as that of two-level type topologies.In this chapter, a new AC-DC SSPFC PWM multilevel converter is proposed. The basic operation of the converter is explained as are the various modes of operation that the converter goes through during a switching cycle. The steady-state characteristics of the converter are determined by mathematical analysis and are used to develop a procedure for the design of key converter components. The feasibility of the new converter is confirmed with results that were obtained from an experimental prototype.

III. A NEW SINGLE-PHASE SINGLE-STAGE THREE-LEVEL POWER FACTOR CORRECTION AC-DC CONVERTER

One of the new AC-DC multilevel SSPFC converters that is proposed in this work is shown in Fig 3.1. The proposed converter is a novel, efficient and cost effective single phase voltage-fed SSPFC that can operate with universal input voltage range (90– 265 V_{rms}) with wide output load variation (from 10% of full load to a full load that is greater than 500 W), fixed frequency PWM control, excellent power factor, a continuous output inductor current for load more than 50%, without its components being exposed to excessive peak voltage stresses. This combination of features does not exist in the present power electronics literature.

A. Operation of the proposed converter

The proposed converter, shown in Fig.1, consists of an AC input section, a three level DC-DC converter, and dc link circuitry that is based on auxiliary windings taken from the main power transformer and that contains an inductor Lin and two diodes. The dc link circuit acts like the boost switch in an AC-DC PFC boost converter. Whenever two converter switches are ON, a voltage is impressed across each auxiliary winding so that the voltage across one of the windings

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cancels out the voltage across the dc link capacitors (sum of the voltage across C1 and C2). This is analogous to the boost switch being ON and current in Lin (which can be considered to be the boost inductor) rises. Whenever only one converter switch is ON, no voltage is impressed across any of the auxiliary windings so that there is no voltage cancellation of the dc link voltage.

The dc link circuit acts like the boost switch in an AC-DC switches are ON, a voltage is impressed across each auxiliary winding so that the voltage across one of the windings cancels out the voltage across the dc link capacitors (sum of the voltage across *C*1 and *C*2). This is analogous to the boost switch being ON and current in *L*in (which can be considered to be the boost inductor) rises. Whenever only one converter switch is ON, no voltage is impressed across any of the auxiliary windings so that there is no voltage cancellation of the dc link voltage. This is analogous to the boost switch being OFF and current in *L*in falls. If the converter is designed so that it operates with a constant duty cycle and a discontinuous *L*in current throughout the line cycle, then input PFC can be achieved without introducing any significant low frequency component to the output as the peak current in *L*in tracks the sinusoidal wave shape of the rectified supply voltage.

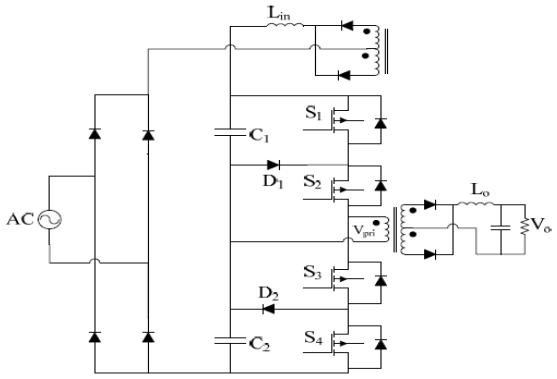

Fig 1 Proposed single-stage three-level converter.

This is analogous to the boost switch being OFF and current in Lin falls. If the converter is designed so that it operates with a constant duty cycle and a discontinuous Lin current throughout the line cycle, then input PFC can be achieved without introducing any significant low frequency component to the output as the peak current in Lin tracks the sinusoidal wave shape of the rectified supply voltage.Typical converter waveforms are shown in Fig 2, and equivalent circuit diagrams that show the converter's modes of operation are shown with the diode rectifier bridge output replaced by a rectified sinusoidal source and thick lines representing the paths of current conduction. The converter has the following modes of operation.

B. Modes of Operation

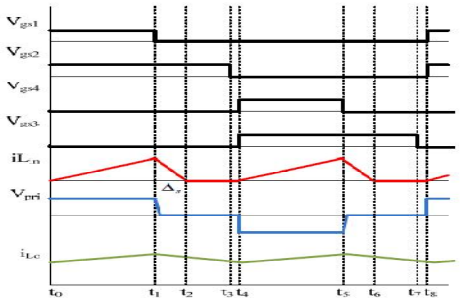

Fig .2 Typical waveforms describing the modes of operation.

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Mode 1 ($t_0 \leq t \leq t_1$):

During this mode1, shown in Fig.3 switches S1 and S2 are ON and energy from the dc-link capacitor *C*1 flows to the output load. Since the auxiliary winding generates a voltage that is equal to the total dc-link capacitor voltage (sum of *C*1 and *C*2), the voltage across the auxiliary inductor is the rectified supply voltage. This allows energy to flow from the ac mains into the auxiliary inductor during this mode.

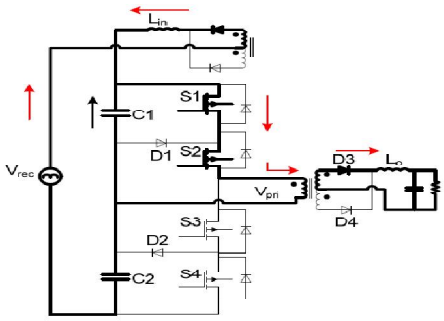

Fig 3.Mode 1 ($t_0 < t < t_1$)

Mode 2 ($t_1 \leq t \leq t_2$):

S1 is OFF and S2 is ON during this mode 2, shown in Fig 4. The energy stored in L_{in} during the previous mode is completely transferred into the dc-link capacitor. The amount of stored energy in the auxiliary inductor depends upon the rectified supply voltage. This mode is a freewheeling mode as the primary current freewheels through S2 and*D*1 and the output inductor current freewheels through both secondary diodes. This mode ends when the current in L_{in}, i_{Laux}, reaches zero.

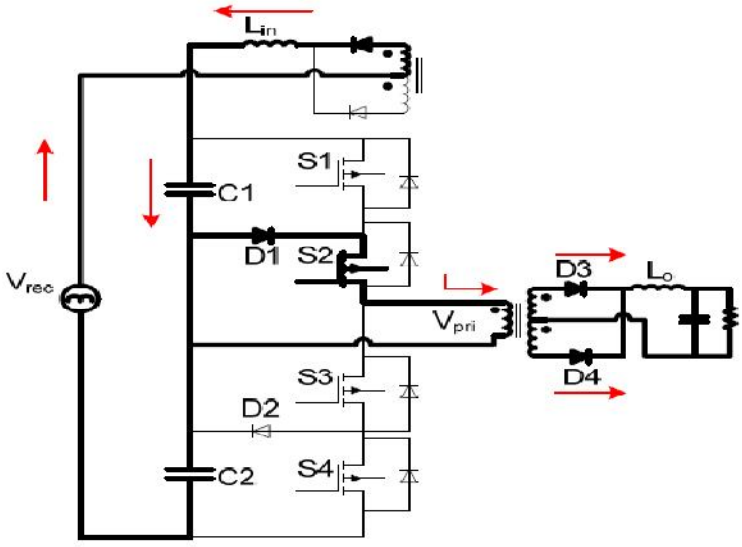

Fig 4. Mode 2 ($t_1 < t < t_2$)

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Mode 3 ($t_2 \leq t \leq t_3$):

Mode 3 is shown in Fig. 5. During this mode S2 is the only switch that is ON. There is no current flowing through L_{aux} and the converter remains in a freewheeling mode

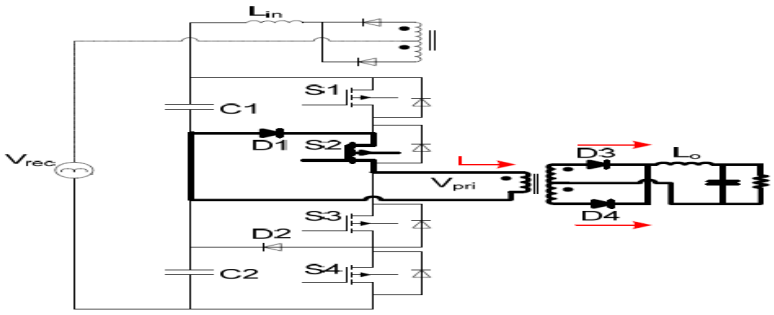

Fig 5 Mode 3 ($t_2 < t < t_3$)

Mode 4 ($t_3 \leq t \leq t_4$):

No converter switch is ON during this mode as the current in the transformer primary charges capacitor *C*2 through the body diodes of S3 and S4. This mode ends when switches S3 and S4 are switched on and a symmetrical half-period begins. The output inductor current continues to freewheel in the secondary of the transformer during this mode. Mode 4 is shown in Fig.6

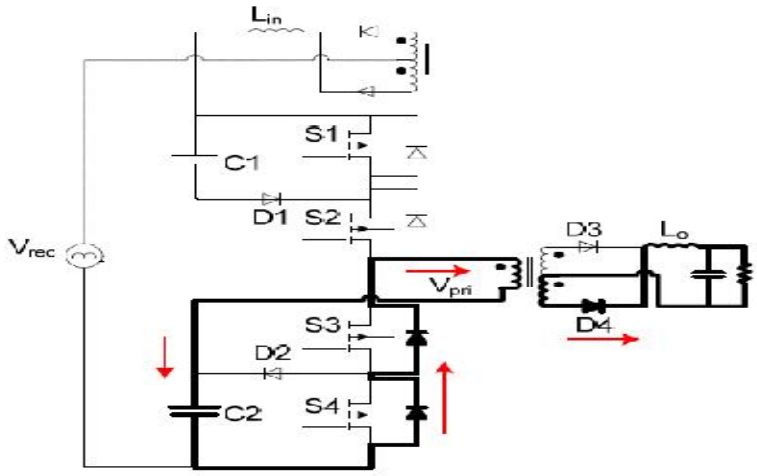

Fig 6. Mode 4 ($t_3 < t < t_4$)

Mode 5($t_4 \leq t \leq t_5$):

This mode is the same as Mode 1 except that S3 and S4 are ON and energy flows from capacitor *C*2 into the load. Mode 5 is shown in Fig.7.

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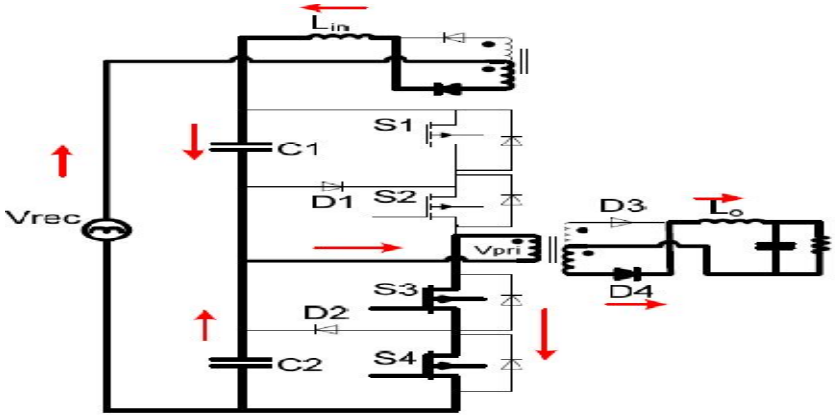

Fig 7. Mode 5 ($t_4 < t < t_5$)

Mode 6 ($t_5 \le t \le t_6$):

This mode is the same as Mode 2 except that S3 is ON. Mode 6 is shown in Fig.6.

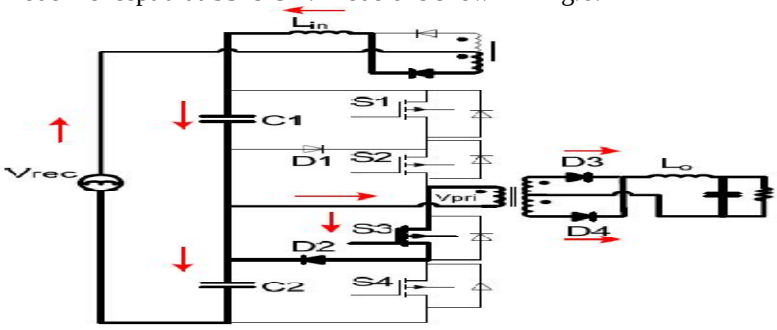

Fig 8. Mode 6 ($t_5 < t < t_6$)

Mode 7 ($t_6 \le t \le t_7$):

This mode is the same as Mode 3 except that the primary current circulates through S3 and diode *D*2. Mode 7 is shown in Fig. 9.

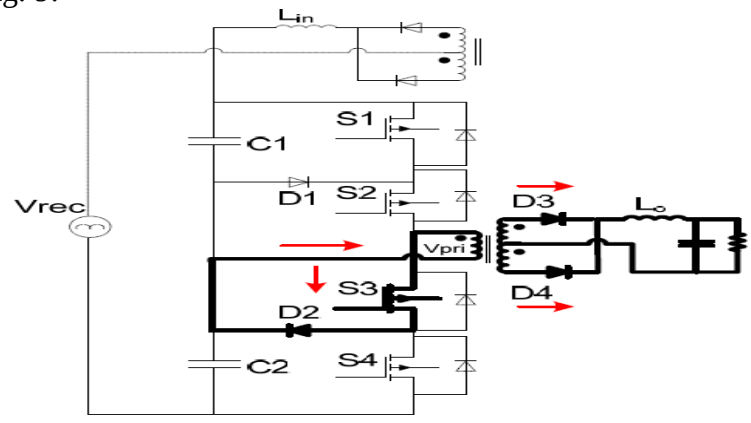

Fig 9 .Mode 7 ($t_6 < t < t_7$)

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Mode 8 ($t_7 \leq t \leq t_8$):

This mode is the same as Mode 1 except that the current in the primary of the transformer charges capacitor *C*1 through the body diodes of S1 and S2. This mode ends when the S1 and S2 are turned ON and the converter re-enters Mode 1. Mode 8 is shown in Fig.10

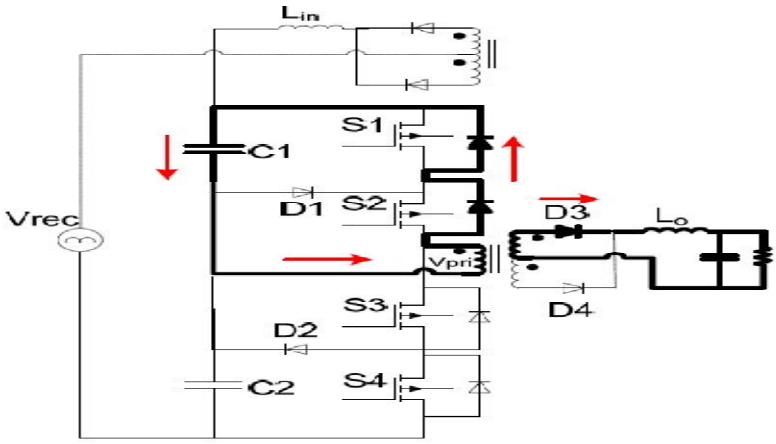

Fig 10. Mode 8 ($t_7 < t < t_8$)

C. Features of the proposed converter:

The Proposed converter has the following features**:**

- The converter can operate with universal input voltage range (90– 265 Vrms) with wide output load variation
- The converters provide high power factor at input ac line current that complies with the IEC1000-3-2. It is because it can have higher dc bus voltage.
- The converter can operate with continuous output inductor current for load more than 50% without its components being exposed to excessive peak voltage stresses.
- The voltage stress for each switch is just half of the dc bus voltage due to multilevel structure.

D. Balancing of dc bus capacitors:

It should be noted that since the converter is a multilevel converter, that the dc bus voltage can be split equally among the capacitors so that the capacitors and the converter switches are not exposed to the full dc bus voltage, but are exposed to half of it. This allows for greater flexibility in the design of the converter as there is less need to constrain the dc bus voltage, as will be shown in the next section. It is the greater flexibility in the converter design that allows for improvements in the performance of a single-stage full-bridge converter.

Since the converter is a multilevel converter, it should be implemented with some sort of capacitor voltage balancing technique to ensure that the voltage across each bus capacitor is the same. Various such techniques have been proposed in the literature, including techniques that sense the capacitor voltages and adjust the duty cycle of the converter switches appropriately. For this work, an auxiliary circuit that is composed of a transformer with a turns ratio of $N_{aux1}/N_{aux2}= 1$ and two diodes D_{aux1} and D_{aux2} was used, as shown in Fig 11. This circuit is very simple, small, and handles only a small fraction of the overall power that is processed by the converter. It should be noted that any other voltage balancing technique could have been used.

The basic principle behind the auxiliary circuit is that if the voltage across one capacitor begins to be greater than the other by more than a diode drop, then one of the diodes begins to conduct as energy is transferred away from the capacitor with the higher voltage. Since the auxiliary circuit does not allow for large differences in bus capacitor voltage, the amount of energy that needs to be transferred away at any given time is small. When the auxiliary circuit is added to the main circuit, it is most likely to come into play during Modes 1 and 5 of operation as this is when the most current will flow through one of the bus capacitors. The auxiliary circuit works as follows during these modes:

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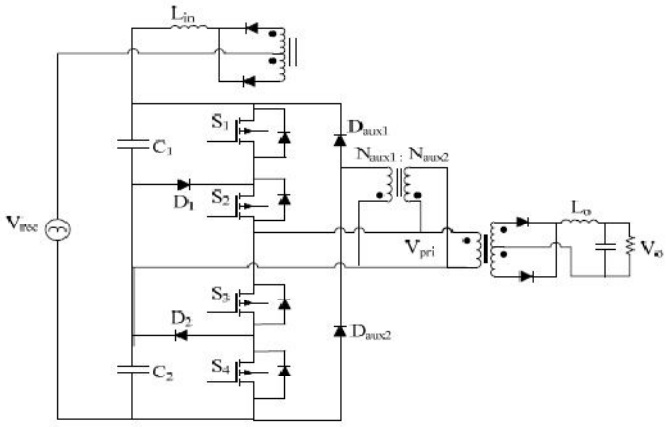

Fig 11.Proposed single-stage three-level converter with auxiliary circuit.

Mode 1 ($t_0 < t < t_1$):

During this mode, switches S1 and S2 are ON and energy from the dc-link capacitor C1 flows to the output load. Since the auxiliary winding generates a voltage that is equal to the total dc-link capacitor voltage (sum of C1 and C2), the voltage across the auxiliary inductor is the rectified supply voltage. This allows energy to flow from the ac mains into the auxiliary inductor during this mode, and the auxiliary inductor current increases. At the beginning of this interval, if there exists any unbalance between the voltages of the two dc-bus capacitors, such that VC1> VC2, the auxiliary circuit starts conducting through diode D_{aux2} to balance the voltage difference across C1 and C2. Fig 13 shows mode 1 with auxiliary circuit.

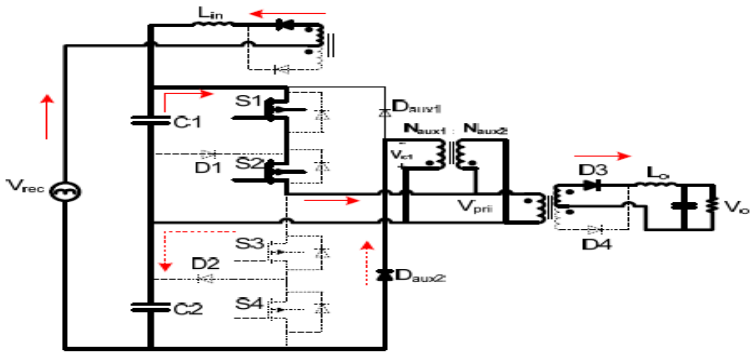

Fig 12.Mode 1 with auxiliary circuit.

Mode 5($t_4 < t < t_5$):

This mode is the same as Mode 1 except that S3 and S4 are ON and energy flows from capacitor C2 into the load. Similarly, in Mode 5, when VC2> VC1, the auxiliary circuit starts conducting through diode D_{aux1} to balance the voltage difference across the capacitors. Fig 13 shows mode 5 with auxiliary circuit.

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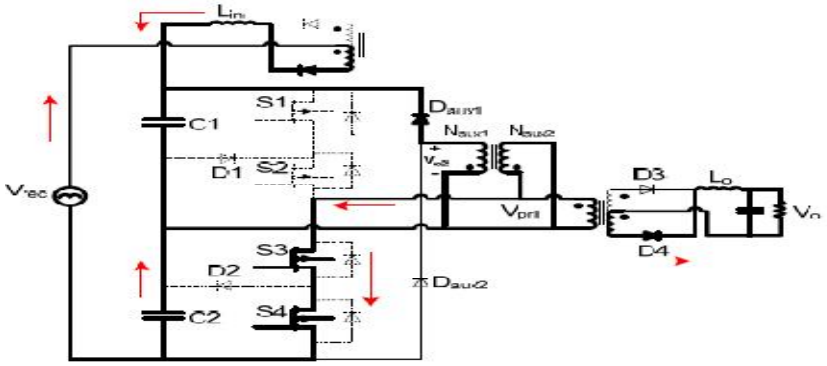

Fig 13.Mode 5 with auxiliary circuit.

It should be noted that since the converter is a multilevel converter, that the dc bus voltage can be split equally among the capacitors so that the capacitors and the converter switches are not exposed to the full dc bus voltage, but are exposed to half of it. This allows from greater flexibility in the design of the converter as there is less need to constrain the dc bus voltage, as will be shown in the next section of this paper. It is the greater flexibility in the converter design that allows for improvements in the performance of a single-stage full-bridge converter.

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The basic principle behind the auxiliary circuit is that if the voltage across one capacitor begins to be greater than the other by more than a diode drop, then one of the diodes begins to conduct as energy is transferred away from the capacitor with the higher voltage. Since the auxiliary circuit does not allow for large differences in bus capacitor voltage, the amount of energy that needs to be transferred away at any given time is small. When the auxiliary circuit is added to the main circuit, it is most likely to come into play during Modes 1 and 5 of operation as this is when the most current will flow through one of the bus capacitors

IV. SIMULATION AND RESULTS

A. SIMULATION CIRCUIT OF CONVENTIONAL CONVERTER

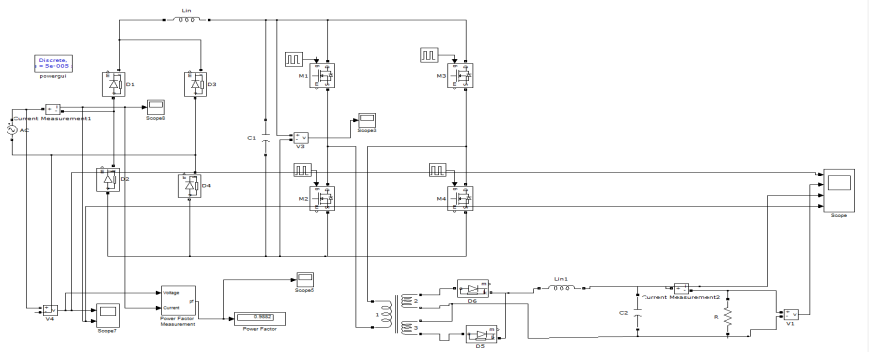

Fig 14.Simulation circuit of conventional two stage converter

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B. SIMULATION RESULTS OF CONVENTIONAL CONVERTER

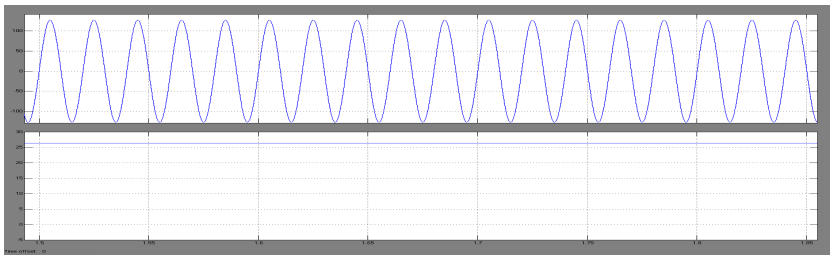

Fig 15.Input and output voltage of conventional circuit

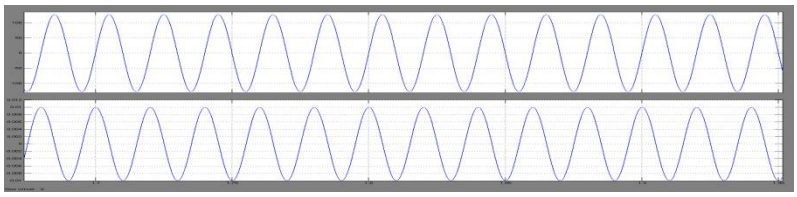

Fig 16.Input voltage and current of conventional circuit

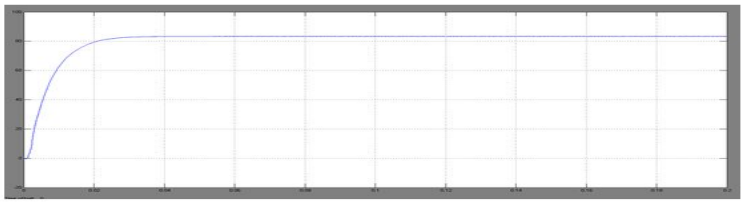

Fig 17.DC bus voltage of conventional circuit

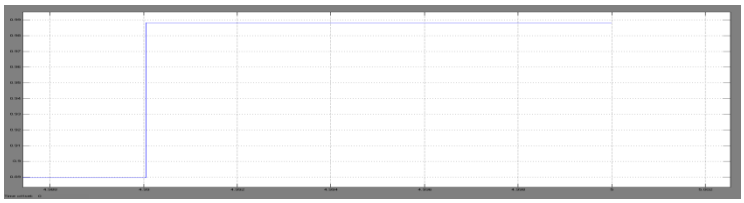

Fig 18 Power factor of conventional circuit

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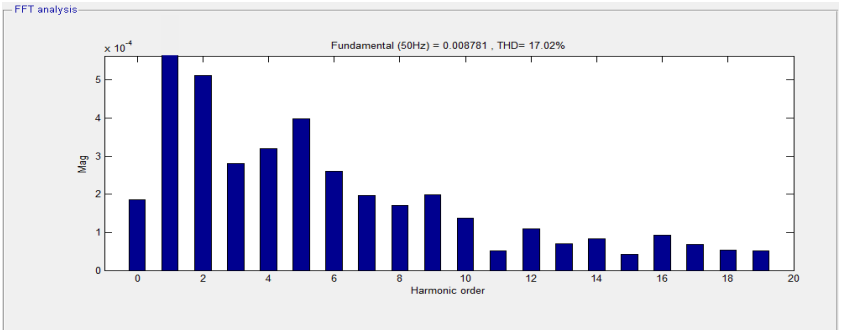

Fig 19. Total harmonic distortion of conventional circuit

C. Proposed single-stage three-level converter circuit.

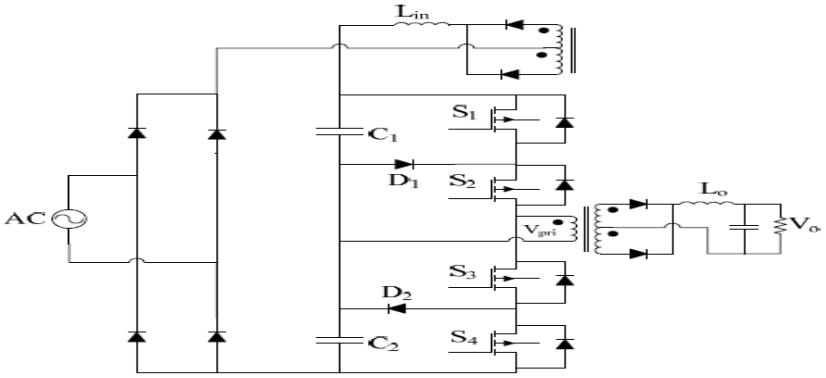

Fig 20. Proposed single-stage three-level converter

D. Simulation circuit of proposed converter

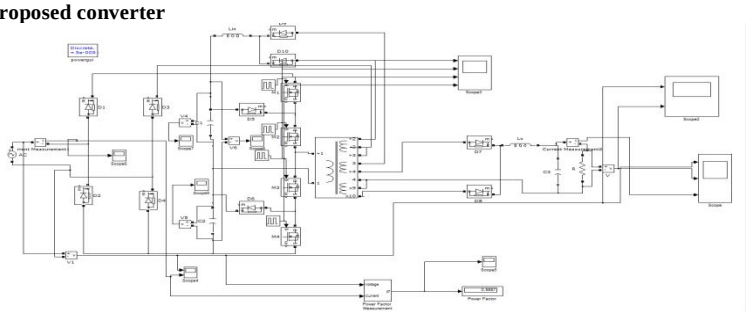

Fig 21. Simulation circuit proposed single stage three-level converter.

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E. **Simulation results of proposed converter**

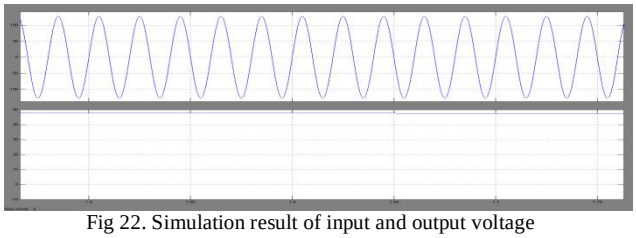

Fig 22. Simulation result of input and output voltage

Fig 23.Triggering pulses

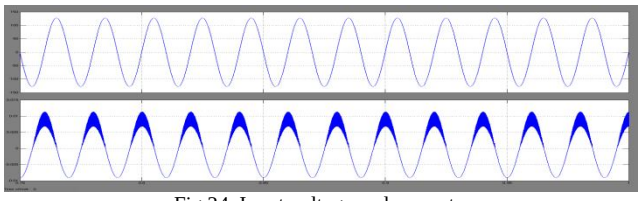

Fig 24. Input voltage and current

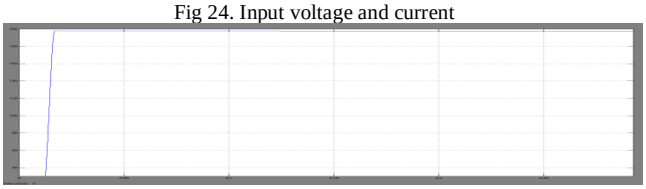

Fig 25. DC bus voltage

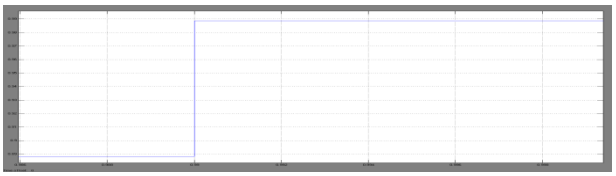

Fig26.Simulation result of power factor

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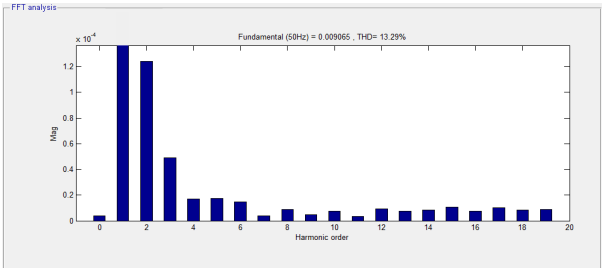

Fig 27. Total harmonic distortion of the proposed circuit

V. CONCLUSIONS

A new three-level, voltage-fed, single-stage, single-phase, power-factor-corrected (SSPFC) AC/DC PWM converter that operates with a single controller was presented. The proposed converter can operate with universal input voltage (90– 265 Vrms) and with a better efficiency, less distorted input current and wider load operating range than previously proposed SSPFC converters. The advantageous features of the proposed converter are due to the fact that it is a three-level converter that allows the uncontrolled primary-side dc bus voltage to be higher than what can be allowed for two-level converters. Hence from the outputs of the conventional two stage converter and proposed single stage converter it is clear that power factor is improved and the total harmonic content is reduced with the proposed one. The power factor obtained in conventional two stage converter is 0.9769 where as in proposed circuit is 0.9887. The Total harmonic distortion value attained in conventional one is 17.02% where as in proposed is 13.29%.

SCOPE OF FUTURE WORK

The single-stage AC-DC converters proposed in the thesis operate with hard switching. No attempt was made to maximize converter efficiency by using any zero voltage switching or zero-current switching techniques to reduce switching losses. Research can be done to investigate the use of such techniques to improve converter efficiency to see how effective these techniques are and to see which techniques are the most effective.

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