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A New Circuit Model of Small-Signal Amplifier using JFETs in Darlington pair Configuration

Dr. SachchidaNand Shukla[1], Susmrita Srivastava[2]

Associate Professor[1], Department of Physics & Electronics, Dr. R. M. L. Avadh University, Faizabad, U.P., India

Research Scholar[2], Department of Physics & Electronics, Dr. R. M. L. Avadh University, Faizabad, U.P., India

ABSTRACT: A small-signal amplifier with two identical JFETs in Darlington pair is proposed and qualitatively analyzed perhaps for the first time. Unlike CS-JFET amplifiers, the voltage gain of this amplifier is significantly higher than unity. In addition, this amplifier can also be tuned in the specific range of audible frequency extended from 90Hz to 19KHz. Tuning performance makes this amplifier suitable to use in Radio and TV receivers. An additional biasing resistance R_A, ranging in 3KΩ to 1MΩ, is to be essentially used in the proposed circuit to maintain its voltage/current amplification property. With this additional biasing resistance, the proposed amplifier crops considerably wide bandwidth (12.365MHz), significantly high current gain (530.909) and fairly high voltage gain (9.108) in 1-80mV input signal range at 1 KHz frequency. These properties offer a flexible application range to the proposed amplifier as high power gain, wide band, or tuned amplifier in permissible audio-frequency range. Variations in voltage gain as a function of frequency and different biasing resistances, temperature dependency of performance parameters, bandwidth and total harmonic distortion of the amplifier are also perused to provide a wide spectrum to the qualitative studies.

Keywords: Small-signal amplifiers, Darlington pair, JFET Darlington pair, RC coupled amplifiers

I. INTRODUCTION

To amplify signals through Darlington pair is an important phenomenon of electronics [1]-[3]. This paired unit of vital importance conventionally holds two identical BJTs in CC-CE connection and its application range is virtually extended from small-signal amplifiers to power amplifier circuits [1]-[3]. Principally, with high input resistance, low output resistance and voltage gain just greater than unity, the current gain factor of Darlington pair (β_D) is treated as identical to the product of current gains of the individual transistors ($\beta_D \approx \beta_{Q1}.\beta_{Q2}$) [1], [3]. However, as a major drawback, its frequency response exhibits a problem of poor response at higher frequencies [1]-[4]. A number of modifications in Darlington's composite unit or in respective amplifier circuits are suggested by researchers to overcome this problem [2], [4]-[6]. These efforts include the use of devices other than BJTs or hybrid combination of active devices (e.g. BJT-JFET or BJT-MOSFET etc.) in Darlington's topology and, moreover, using some additional biasing components in associated amplifier circuit [7]-[10]. Experimentation with Darlington pair topology is still a popular topic for electronic circuit designers to work with [2],[6],[11]-[12].

Present investigation is focused around a Darlington pair which uses two identical JFETs in its composite unit. This pair with appropriate biasing component is explored as new circuit model of a small-signal amplifier suitable for radio and TV receiver stages.

II. CIRCUIT DETAILS

Present work comprises a qualitative comparison between small-signal conventional Darlington pair amplifier (Fig.1) and a new circuit of small-signal amplifier which is having identical JFETs in Darlington pair configuration (Fig.2) and an additional biasing resistance in the circuit.

Conventional Darlington pair amplifier [1]-[2],[4],[6],[11] of Fig.1 is named as Reference Amplifier for the present studies whereas the Proposed Amplifier circuit of Fig.2 is obtained by replacing paired BJTs of the circuit of Fig.1 with that of identical JFETs. In addition, the proposed amplifier circuit also uses an additional biasing resistance R_A [2],[4],[6] between source of J1 and ground. Amplifier circuits under discussion use potential divider biasing methodology [4],[6]-[7] with properly selected passive biasing components. Component details of respective circuits are summarized in TABLE I.

PSpice simulation (Student version 9.2) is performed to carry out present investigations [15]. Observations are procured by feeding the amplifier circuits with 1V AC input signal source, from which, a small-distortion-less AC signal of 1mV for reference amplifier (Fig.1) and 30mV for proposed amplifier (Fig.2) at 1KHz frequency is drawn as input for the amplification purpose.

Amplifiers of Fig.1 and Fig.2 provide fair and distortion-less results in 1-10mV and 1-80mV range of AC input signals respectively at 1KHz frequency. However the best results for reference and proposed amplifiers are received at 1mV and 30mV AC inputs respectively.

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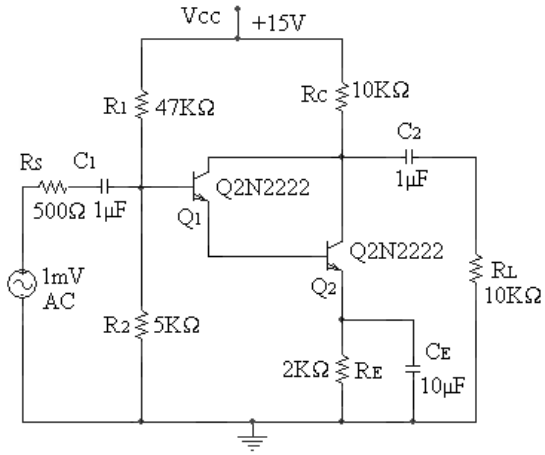

Fig.1. Reference Amplifier (Conventional Darlington pair amplifier)

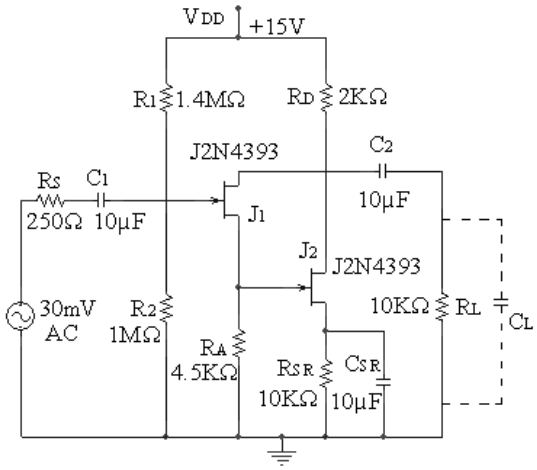

Fig.2. Proposed Amplifier (JFET Darlington pair amplifier)

TABLE I
COMPONENT DETAILS OF THE CIRCUITS UNDER DISCUSSION

COMPONENTS	COMPONENTS DESCRIPTION	REFERENCE AMPLIFIER	PROPOSED AMPLIFIER
Q1	NPN BJT (β=255.9)	Q2N2222	-
Q2	NPN BJT (β=255.9)	Q2N2222	-
J1	N-Channel JFET (V_{TH}= -1.422)	-	J2N4393
J2	N-Channel JFET (V_{TH}= -1.422)	-	J2N4393
R_S	Source Resistance	500Ω	250Ω
R_1	Biasing Resistance	47KΩ	1.4MΩ
R_2	Biasing Resistance	5KΩ	1MΩ
R_D/R_C	Drain/Collector Biasing Resistance	10KΩ	2KΩ
R_{SR}/R_E	Source/Emitter Biasing Resistance	2KΩ	10KΩ
R_A	Added Biasing Resistance	NA	4.5KΩ
R_L	Load Resistance	10KΩ	10KΩ
C_1, C_2	Coupling Capacitors	1 μF	10μF
C_S/C_E	Source/Emitter By-pass Capacitor	10μF	10μF
DC Biasing	DC Biasing Supply	+15V DC	+15V DC
AC input signal	AC input signal range for purposeful amplification	1-10mV (1KHz)	1-80mV (1KHz)

III. OBSERVATIONS AND DISCUSSIONS

A. Qualitative Performance

Fig.3 depicts the variation of voltage gain as a function of frequency. At biasing parameter values of TABLE I, the reference amplifier produces 16.98 maximum voltage gain A_{VG} (with 17.328mV peak output voltage), 8.51 maximum current gain A_{IG} (with 1.7327μA peak output current) and 102.058KHz bandwidth B_W (with f_L=79.913Hz and f_H=102.138KHz) [1]-[2],[4],[6],[11] whereas the proposed amplifier generates 9.1084 maximum voltage gain A_{VG} (with 269.696mV peak output voltage), 530.909 maximum current gain A_{IG} (with 26.971μA peak output current) and 12.365MHz bandwidth B_W (with f_L=88.207Hz and f_H=12.366MHz). In addition, if values of coupling capacitors C_1 and C_2 are reduced to 0.1uF, the bandwidth of the proposed amplifier enhances nominally to reach at 12.548MHz whereas A_{IG} reduces to 526.883 with almost no change in A_{VG}. Though the observed value of A_{VG} of the proposed amplifier is less than reference amplifier but this amount is still significant for small-signal JFET amplifiers. In addition, the proposed amplifier also crops considerably wide bandwidth and high current gain and successfully removes the poor-response-problem of conventional Darlington pair amplifier (Fig.1) at higher frequencies.

Both the amplifiers of Fig.1 and Fig.2 invert phase of voltage or current in amplification mode [1]-[2],[13]. In fact, BJTs in paired unit of reference amplifier hold CC-CE configuration and a CC configuration independently do not show any phase shift between applied input and amplified output signals whereas CE configuration produces an amplified output having 180^o phase difference with input. Therefore the resultant paired unit of CC-CE BJTs reverts the phase of output waveform. The similar situation appears for proposed amplifier which holds a CD-CS configuration of JFETs with a property that CD configuration does not reverses the phase whereas CS configuration inverts the phase of output waveform in amplification process.

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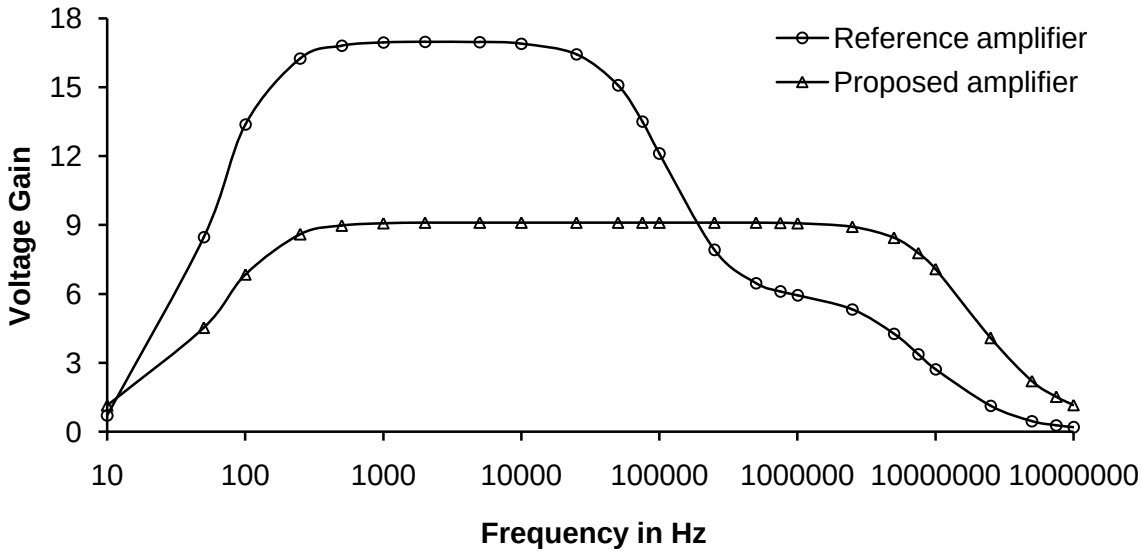

Fig.3. Voltage gain as a function of frequency

Variation of A_{VG}, A_{IG} and bandwidth with temperature for both the amplifiers is also measured and listed in TABLE II. Bandwidth of the reference amplifier remains unchanged whereas both varieties of gains increase with rising temperature. However, bandwidth of the proposed amplifier mildly increases but voltage and current gains significantly decrease at rising temperature. This decrement in A_{IG} and A_{VG} is associated with 'negative temperature coefficient' property of drain current [13]. The drain current in JFET is mainly composed of majority carriers whose mobility decreases at elevated temperature due to enhanced collision rate between them and the remaining ions in the semiconductor channel [13]. This decreases the drain current and therefore the effective current and voltage gain of the JFET based Darlington pair system.

TABLE II
VARIATION OF A_{VG}, A_{IG} AND BANDWIDTH B_W WITH TEMPERATURE

Temperature (°C)	Reference Amplifier (Fig.1)			Proposed amplifier (Fig.2)		
	Maximum voltage gain A_{VG}	Maximum current gain A_{IG}	Bandwidth (KHz)	Maximum voltage gain A_{VG}	Maximum current gain A_{IG}	Bandwidth (MHz)
-30	8.95	4.48	102.06	10.37	604.55	11.95
-20	10.55	5.29	102.06	10.14	590.97	12.03
-10	12.07	6.05	102.06	9.91	577.68	12.10
0	13.51	6.77	102.06	9.68	564.67	12.17
10	14.86	7.45	102.06	9.47	551.94	12.24
27	16.98	8.51	102.06	9.11	530.91	12.36
50	19.53	9.79	102.06	8.64	503.65	12.53
80	22.38	11.22	102.06	8.06	470.08	12.63

Performance of the proposed amplifier highly depends on the presence of additional biasing resistance R_A. Variation of maximum voltage and current gains with R_A is also observed but results are not shown in form of graphs. It is noticed that the proposed amplifier with R_A=3KΩ crops A_{IG}=378.427 and A_{VG}=6.4925 which climbs-up to A_{IG}=546.817 and A_{VG}=9.3786 at R_A=1MΩ. This happens because on increasing R_A, the gate potential of J2 increases and allows N-type channel to bear a flow of more majority carriers which causes an enhancement in drain current and therefore the load current and current gain. If R_A is removed from the proposed circuit, the A_{IG} of the amplifier reaches below unity to a value 0.487 whereas A_{VG} to a non-significant value of 0.118. Conclusively, the presence of additional biasing resistance R_A in the proposed configuration is essential to establish 'JFET Darlington pair unit' suitable for amplification of small-signals.

The input and output noises for proposed amplifier at 100Hz, 1KHz and 1MHz frequencies are observed and respective values are listed in TABLE III. Usually, resistors and semiconductor devices in electronic circuits are responsible to generate noises during amplification process. Table clearly indicates that levels of input and output noises are significantly low for proposed amplifier and within the permissible limit. Both varieties of noises reduce with elevation of operating frequency. Moreover, it also increases with temperature which is an obvious feature due to generation of more carriers and their higher collision rate at elevated temperature.

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TABLE III
VARIATION OF INPUT AND OUTPUT NOISES WITH TEMPERATURE FOR PROPOSED AMPLIFIER

Temperature (^{O}C)	Total Output Noise (Volts/√Hz)			Total Input Noise (Volts/√Hz)		
	100Hz ($x10^{-8}$)	1KHz ($x10^{-8}$)	1MHz ($x10^{-8}$)	100Hz ($x10^{-9}$)	1KHz ($x10^{-9}$)	1MHz ($x10^{-9}$)
-30	5.490	3.418	2.532	7.480	3.312	2.449
-20	5.568	3.428	2.539	7.669	3.396	2.513
-10	5.641	3.436	2.545	7.862	3.482	2.576
0	5.713	3.443	2.549	8.060	3.569	2.639
10	5.783	3.448	2.551	8.261	3.656	2.703
27	5.901	3.455	2.552	8.615	3.808	2.811
50	6.055	3.460	2.547	9.115	4.018	2.957
80	6.246	3.459	2.533	9.808	4.303	3.150

Total Harmonic Distortion (THD) percentage is also calculated for 8 significant harmonic terms using established rules [1],[12],[16]. It is found that the reference amplifiers shows 0.72% THD whereas the proposed amplifier shows 2.15% THD. THDs of both the amplifiers can be significantly reduced by increasing load resistance R_L, but this simultaneously reduces the voltage and current gains of the respective amplifiers. TABLE IV shows A_{VG}, A_{IG} and THD at increasing values of Load Resistance R_L.

TABLE IV
VARIATION OF A_{VG}, A_{IG} AND THD% WITH R_L

R_L	Reference Amplifier (Fig.1)			Proposed Amplifier (Fig.2)		
	THD%	A_{VG}	A_{IG}	THD%	A_{VG}	A_{IG}
1KΩ	0.74	2.13	15.69	2.39	3.68	2148.2
10KΩ	0.72	16.98	8.52	2.15	9.11	530.91
20KΩ	0.62	22.53	5.65	2.14	9.91	289.06
100KΩ	-	-	-	2.12	10.67	62.24

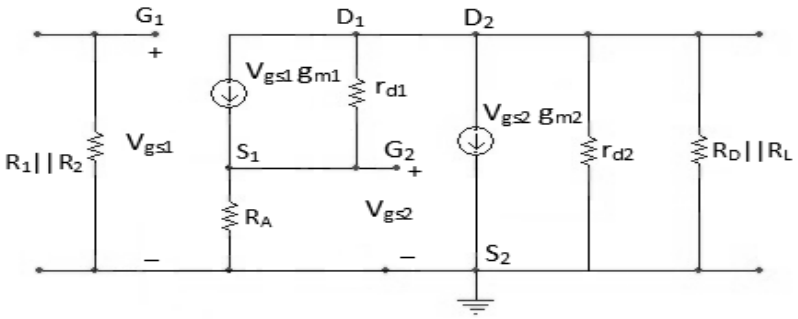

Fig.4. AC equivalent circuit of proposed amplifier

Small-signal AC equivalent circuit of proposed amplifier is drawn in Fig.4. AC analysis of this amplifier shows that its equivalent output resistance $R_O \approx R_L \| R_D$ is lower (≈1.66KΩ) than the equivalent input resistance $R_I \approx R_1 \| R_2$ (≈0.58MΩ), with a phase reversal in output voltage waveform. In addition, AC voltage gain of the proposed amplifier is estimated to be the following-

$$A_V = -\frac{g_{m1}}{\frac{1}{r_{d2}} + \frac{1}{r_{d1}} - \frac{1}{R_o} - \frac{\left[\frac{1}{r_{d1}} - g_{m2}\right]\left[\frac{1}{R_o} - \frac{1}{r_{d2}}\right]}{\left[g_{m2} + \frac{1}{R_A}\right]}}$$

and therefore figured out to be -14.076 [1] which is approximately five point higher than the observed value. Here the computed r_{d1}=1.77KΩ, r_{d2}=2.06KΩ, g_{m1}=0.0077mho and g_{m2}=0.0055mho. Negative sign in the expression shows phase reversal of the output voltage which is because the composite unit of JFET Darlington pair holds an equivalent CS configuration [1].

Voltage and current gain of the corresponding amplifiers highly depends on Emitter resistance (for reference amplifier) or source resistance (for proposed amplifier). Respective observations are shown in Fig.5. Voltage gain of the reference amplifier is found to decrease exponentially whereas current gain decreases nonlinearly at increasing values of R_E. However, voltage and current gain of the proposed amplifier increases up to 10KΩ, thereafter, decreases exponentially at increasing values of R_{SR}.

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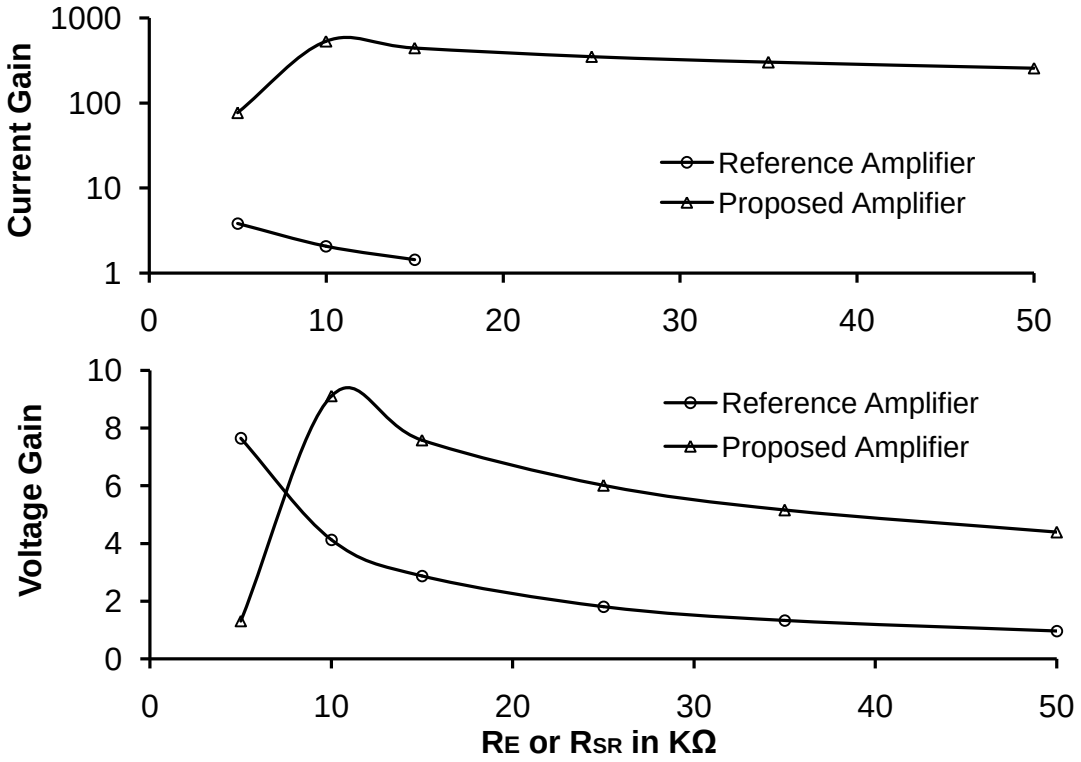

Fig.5. Variation of Maximum voltage and current gains with R_{SR} or R_E

Performance parameters A_{VG}, A_{IG} and B_W at different values of Collector resistance R_C (for reference amplifier) and Drain resistance R_D (for proposed amplifier) are also estimated but not shown graphically. For reference amplifier, respective parameters behave in the similar way as was observed by Tiwari et.al. [4],[6] and Sayed et.al.[2]. However, for proposed amplifier, voltage gain (2.66) and current gain (155.236) are found at lowest but bandwidth (52.089MHz) at highest for R_D=500Ω whereas for R_D=2KΩ voltage gain (9.108) and current gain (530.909) are found at maximum but bandwidth (12.365MHz) at minimum. The proposed amplifier yields a poor response at lower frequencies if R_D is raised beyond critical value of 2KΩ. Performance parameters are also estimated at different values of DC supply voltage V_{CC} for reference and proposed amplifiers but not shown graphically. Observations indicate that the voltage gain (9.10), current gain (10.12) and bandwidth (12.365MHz) for proposed amplifier are found at lowest for V_{CC}=15V whereas for V_{CC}=30V voltage gain (11.91), current gain (694. 07) and bandwidth (14.923MHz) attain their maximum. The proposed amplifier yields a poor response if V_{CC} is raised above 30V or lowered below 15V. Variation of maximum voltage gain with load resistance R_L is also observed but not shown in form of graphs. Observations shows that gain value rises up continuously in low resistance range up to 50KΩ value of R_L whereas at higher R_L values it approaches towards a sustained level. This nature is well in accordance of the basic nature of small-signal amplifiers [2],[6],[16].

B. Tuning Performance

Tunned amplifiers are frequently used in designing Radio or TV receiver type systems [11],[13]. The common practice used to design such amplifiers is to introduce a parallel tuning network (usually L-C-R) at their output or input section. If central frequency of the response is so adjusted to match with the frequency of a particular channel, desired signal can be received. Motayed et.al.[11] had already floated the idea behind tuning of a small-signal CC-CE Darlington pair amplifier (Fig.1), therefore, objective of the present investigation is also to extend the design of proposed amplifier to behave as a successful tuned-amplifier.

The tunning performance of the proposed amplifier is established in two steps- first, with R_{SR}-C_{SR} network available at the source end of J2 (Fig.2) and second by introducing a tunning capacitor C_L across the load R_L (indicated as doted lines in Fig.2). Respective observations are listed in TABLE V.

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TABLE V
VARIATION OF $A_{VG\text{-}MAX}$, $A_{IG\text{-}MAX}$, f_H, f_L AND BANDWIDTH FOR PROPOSED AMPLIFIER WITH TUNING CAPACITOR C_{SR} AND C_L

Tuning performance with source capacitor C_{SR}						Tuning performance with source capacitor C_L					
C_{SR}	f_H (MHz)	f_L	Bandwidth (MHz)	A_{VG}	A_{IG}	C_L	f_H (KHz)	f_L (Hz)	Bandwidth (KHz)	A_{VG}	A_{IG}
						100pF	906.37	88.562	906.282	9.1075	530.680
0.01µF	12.485	87.471KHz	12.397	9.0812	243.733	1nF	96.88	88.181	96.799	9.0993	530.397
0.1µF	12.410	8.8588KHz	12.401	9.1057	474.834	10nF	9.92	86.709	9.832	9.0183	525.833
1µF	12.405	883.823Hz	12.404	9.1082	525.263	50nF	2.05	76.622	1.973	8.6785	506.211
10µF	12.373	88.147Hz	12.372	9.1084	530.909	100nF	1.15	76.771	1.076	8.2822	482.523

Tunning performance of the proposed amplifier with source bypass capacitor C_{SR} is obtained for variations between 0.01µF and 10µF. Changes in the C_{SR} merely create any variation in voltage gain, whereas it significantly changes current gain and plays a prime role in adjusting the mid-bandwidth (e.g. for C_{SR}=0.01µF, bandwidth extends between f_L=87.471KHz and f_H=12.485MHz). Other values of Upper and Lower Cut-off frequencies for different C_{SR} can be observed in TABLE V. It is evident from TABLE V that f_H varies in a non-significant range with C_{SR} whereas f_L considerably shifts towards lower values at increasing C_{SR}.

Similarly the inclusion of capacitor C_L across load resistance R_L also plays an important role in adjusting mid-band frequency range for proposed amplifier. Tunning is obtained for variations of C_L between 100pF and 100nF with a feature that the bandwidth of the amplifier shifts towards lower range (from MHz to KHz range) on the frequency axis. Voltage gain, current gain and lower-cut-off frequency varies in a very short range for corresponding variations in C_L, whereas, the upper-cut-off limit of the bandwidth shifts towards lower values with increasing C_L.

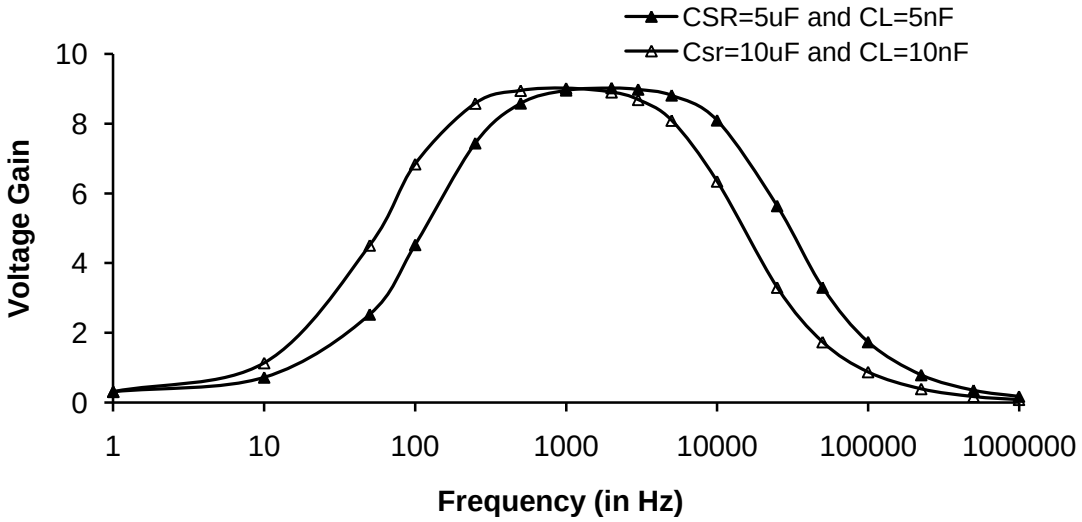

Fig.6. Tuned frequency response of JFET Darlington pair amplifier at two different combinations of C_{SR} and C_L

Conclusively, adjustment of C_{SR} and C_L will lead to a tunning which finally ascertain the frequency response of the proposed amplifier to peak around the desired frequency. This may enable the central frequency of the response to coincide with the frequency of a desired communication channel. This tunning idea is depicted in Fig.6 for two different combinations of C_{SR} and C_L. The explored idea of tuning in Fig.6 leads to a conclusion that CD-CS combination in JFET Darlington pair configuration can be applied to receive signal of a specific channel by filtering-out or attenuating others.

IV. CONCLUSION

As a novel approach, two identical JFETs are used in Darlington pair to explore the proposed circuit as small-signal wide-band amplifier. The proposed amplifier can be tuned in permissible audible frequency range approximately extended from 90Hz to 19KHz. The additional biasing resistance R_A (ranging in between 3KΩ to 1MΩ), is to be essentially included in the proposed circuit to maintain its voltage/current amplification property. In absence of R_A, amplifier's voltage and current gains climbs-down below unity and makes it purpose-less. This amplifier can effectively process small-signals ranging below 80mV in the frequency band of 88.2074Hz to 12.366MHz at 1KHz input frequency and is free from the problem of poor response of conventional small-signal Darlington pair amplifiers at higher frequencies. With sufficiently wide bandwidth, high current gain, and a voltage gain noticeably greater than unity, the proposed amplifier generates only 2.15% harmonic distortion which is fairly adaptive for small-signal amplifiers. Observed values of voltage and current gains logically set the power gain of the proposed amplifier considerably larger

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than unity. Collectively, these features provide a unique flavour to the proposed amplifier in the respective class of JFET based small-signal audio amplifiers. The proposed amplifiers shows a considerable response for V_{CC}, R_{SR}, R_D and R_L almost in the same way as is usually observed for small-signal RC coupled Common Source amplifiers.

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Biography

SachchidaNand Shukla received his M.Sc. and Ph.D. Degrees in Physics (Electronics) from Dr. Ram Manohar Lohia Avadh University, Faizabad in 1988 and 1991 respectively. Presently he is working as Associate Professor in the Department of Physics and Electronics of Dr. Ram Manohar Lohia Avadh University, Faizabad, U.P., India and actively engaged in researches related to the Circuit designing and simulation. During last five years, he published over 33 research papers in International/National journals and Conference Proceedings on various topics of his current research interest.

Susmrita Srivastava received her M.Sc. degree in Electronics from Department of Physics and Electronics of Dr. Ram Manohar Lohia Avadh University, Faizabad, U.P., India in 2008. Presently she is pursuing Ph.D. degree in Electronics and published 15 research papers on various topics of Circuit designing and simulation in International /National journals and Conference Proceedings.