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2GHZ PLL Frequency Synthesizer for Zigbee Applications

Rajesh A. Dabhi, , Bharat H. Nagpara,

Student, Department of ECE, C. U. Shah College of Engineering and Technology, Wadhwan city, Gujarat, India.

Professor, Department of ECE, C. U. Shah College of Engineering and Technology, Wadhwan city, Gujarat, India.

ABSTRACT: - A low power 2GHz PLL frequency synthesizer for Zigbee/IEEE 802.15.4 applications is presented. The current starve VCO is used to decrease power consumption and to improve noise characteristic of the synthesizer. The Synthesizer employs a 1 MHz fully programmable divider with an improved TSPC 2/3 prescaler, a novel bit-cell for the programmable counters and PFD,charge pump and passive loop filter to reduce the PLL reference spurs. The PLL consumes a power of 1.026mW at 1 V power supply with the programmable divider consuming only 613.39 µW. The phase noise of the VCO is – 44.77dBc/Hz at 1 MHz offset.Measured results show that the frequency tuning range is 2.46GHz-2.541GHz and the locking time is 4µs. The synthesizer is design and simulated on Tanner EDA Tool using 45nm CMOS process technology with supply voltage 1 V.

KEYWORDS: Phase locked loop (PLL), True Single Phase Clocked (TSPC), Voltage control oscillator (VCO), Phase frequency detector (PFD, Tanner Tool.

I. INTRODUCTION

ZigBee is an emerging short distance wireless communication technology. It is mainly used for short range, low power consumption and low transfer rate data applications [1] [2]. As an important part of ZigBee wireless communication radio frequency chip, the power consumption of frequency synthesizers occupies a large part of the total consumption of ZigBee chip. The design of low power frequency synthesizer is one of the challenges in Zigbee wireless communication system. This paper proposes a low power CMOS integrated 2GHz PLL frequency synthesizer. The current starve VCO is used to decrease power consumption and to improve noise characteristic of the synthesizer.

The paper is organized as follows: section II, presents some details on the synthesizer architecture. In section III, the simulation results of the PLL implementation are shown and discussed. Conclusions are given in the last section.

II. THE SYNTHESIZER ARCHITECTURE

A. Proposed Synthesizer Architecture

The block diagram of the proposed PLL Frequency synthesizer is shown in Figure.1 [10], [11]. It is N-integer architecture, it comprises one, phase-frequency detectors (PFD), and charge pump (CP), a passive low pass loop filter, current starve VCO, a fully programmable dual-modulus frequency divider with Programmable counter and swallow counter.

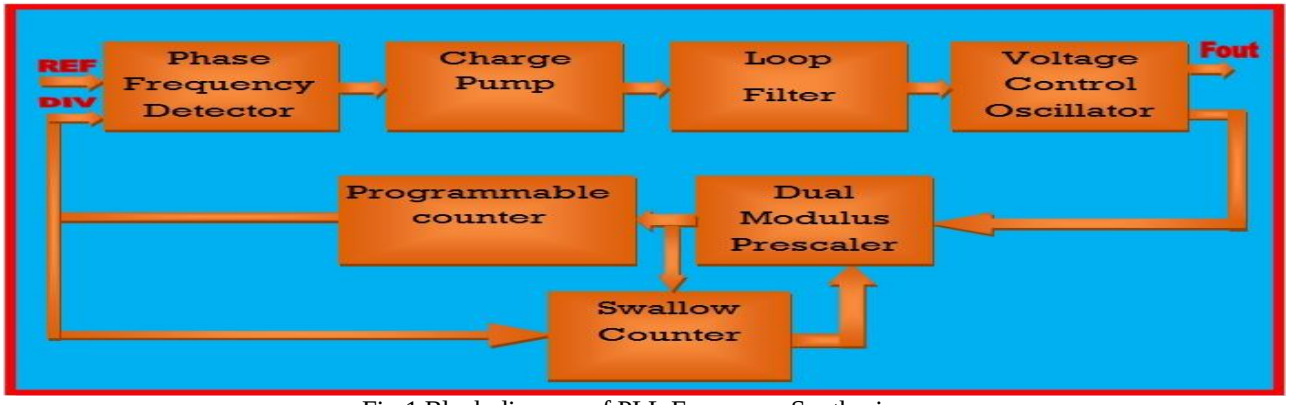

Fig.1 Block diagram of PLL Frequency Synthesizer

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B.Phase Frequency Detector (PFD).

It consists of two edge triggered D flip flops with their D inputs tied to logic 1 and a AND Gate in the reset path. In reset path NAND, NOR gate can be used. PFD compare Ref signal and Div signal. Generate three sequential logic states for controlling Charge Pump. Fig.2 shows the PFD using AND gate. The circuit consists of two edge triggered D flip flops DFF which is resettable, with their D inputs tied to logic 1 and a AND Gate in the reset path [8]. The Ref and Div serve as clocks of the flip flops. Suppose the rising edge of Ref leads that of Div, then UP goes to logic high. UP keeps high until a low to high transition occurs on Div. Because UP and DN, are AND, so Reset goes to logic high and resets the PFD into the initial state.

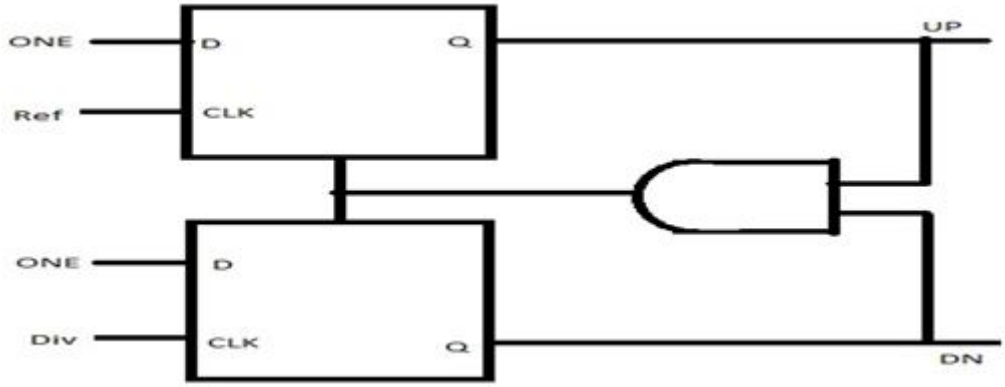

Fig.2 AND Gate based PFD

The PFD is a state machine with three states. When Ref leads Div, the UP output is asserted on the rising edge of Ref. and UP signal goes high.

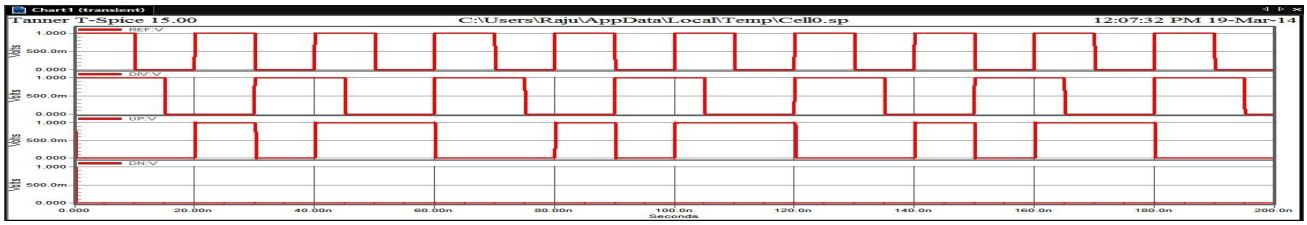

Fig 3. (a) Simulation result when REF lead DIV

In the second case, ref signal is lagging Div signal. In this DN pulse represents the difference between the phases of two clock signals.

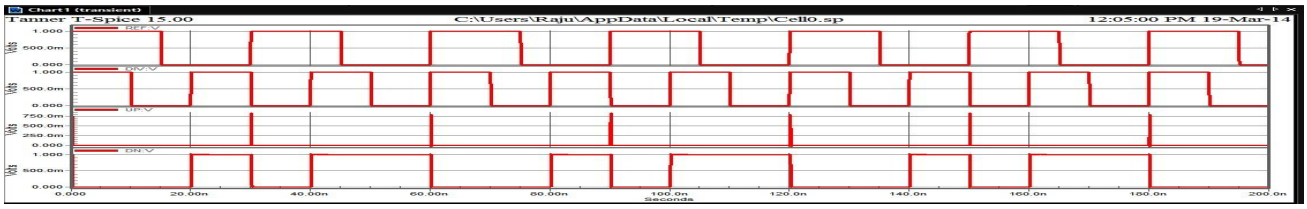

Fig 3. (b) Simulation result when DIV lead REF

In the third case, Ref signal is in phase with Div signal, which is shown in Fig. 3(c). In this case, the loop is in locked state and short pulses will be generated on the up and DN outputs.

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Fig 3. (c)Simulation result when REF = DIV

Figure 3 (a),(b),(c) simulation result of PFD

C. Charge Pump

A charge pump is three state designs. It takes two inputs out from the PFD and outputs a DC current or voltage. The charge pump consists of two current sources and the output of the charge pump drives the low pass filter. The charge pump either charges or discharges a capacitor with voltage or current pulses. A filter is used to limit the rate of change of the capacitor voltage, and the result is a slowly rising or falling voltage that depends on the frequency difference between the PLL output voltage and the reference frequency. The VCO increases or decreases its frequency of operation as the control voltage is increased or decreased. Following figure 4 shows the charge pump [10].

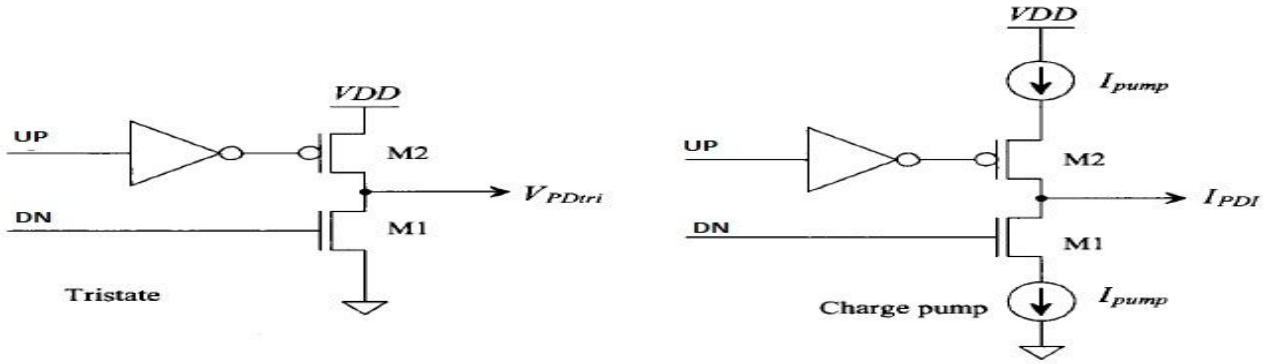

Fig.4 (a) Tri-state and (b) charge pump outputs of the PFD

D.LOOP FITER

The design of the loop filter is the principle tool in selecting the bandwidth of the PLL. A PLL without a loop filter result in a 1st order system. First order system is rarely used as they offer little noise suppression. Since higher order loop filters offer better noise cancelation, loop filters of order 2 and more are used in critical applications, such as in the case of frequency synthesizer. The purpose loop filter is to convert the charge pump current Icp into a voltage controlled signal Vctrl, to filter the alternating current component and to suppress the noise.

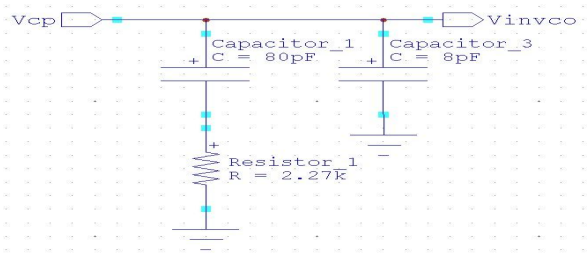

Fig. 4 Loop filter

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Figure 5(a) shows simulation result when Ref signal is leading Div signal. In this DN pulse represents the difference between the phases of two clock signals.it increase charge pump current in such a way that it increase VCO oscillation.

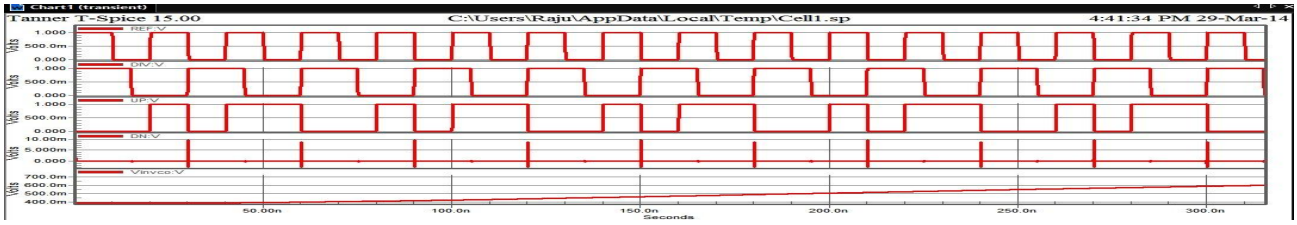

Figure 5(a) Simulation result when REF lead DIV

Figure 5(b) shows simulation result when Ref signal is lagging Div signal. In this DN pulse represents the difference between the phases of two clock signals.it decrease charge pump current in such a way that it decrease VCO oscillation.

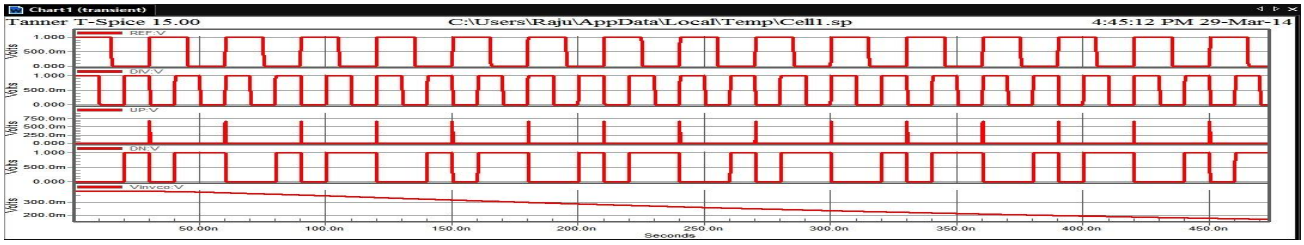

Figure 5(b) Simulation result when DIV lead REF

E. Current Starved VCO.

VCO is a frequency modulated oscillator whose instantaneous output frequency is directly proportional to its control voltage .A ring oscillator can be smoothly integrated in a standard CMOS process without taking extra processing steps because it does not require any passive resonant element compare to CMOS LC-tank oscillator. In this work 5-stage CMOS inverter forms a closed path with positive feedback [10]. The schematic of the whole VCO is shown in fig 1.Voltage control oscillator have a CMOS inverter circuit as shown in figure2.This inverter circuit is connected to current sources M3 and M4 that limit the current available to the inverter. The currents in MOSFETs M1 and M2 are mirrored in each inverter stage.

The oscillation frequency of the current-starved VCO for N (an odd number > 5) of stages is

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{I_D}{N \cdot C_{tot} \cdot VDD}$$

Which is fcenter (@VinVCO = VDD/2 and ID = IDcenter)

Schematic of current starved VCO is shown in figure 6.with 5 stage.

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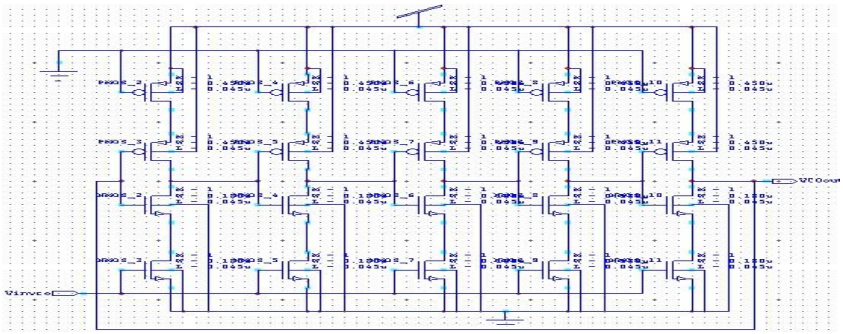

Figure 6. Current Starved VCO

Simulation Result of Current Starved VCO

The transient analysis of current starved VCO is shown in figure 6.1.For input control voltage, Vinvco, equal to 0.50mV, an output frequency of 2.4GHz has been obtained. The input control voltage is varied from 0.1V to 1V, in steps of 0.5V,and output Frequency is observed.

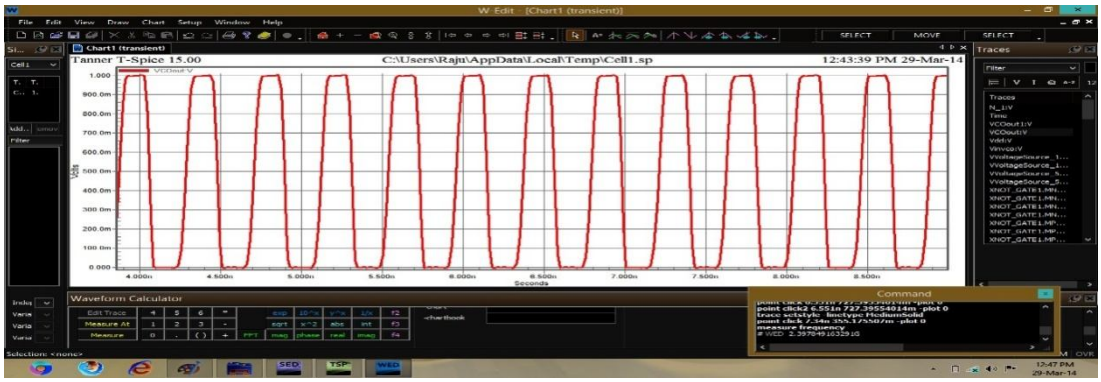

Figure 6.1 Waveform of VCO

The measured tuning range of the VCO is 5.23MHz to5098MHz. As shown in figure 6.2 the plot of the input control voltage versus the output oscillation frequency. It shows that 2.4GHz frequency is obtain at Vinvco equal 0.50mV.

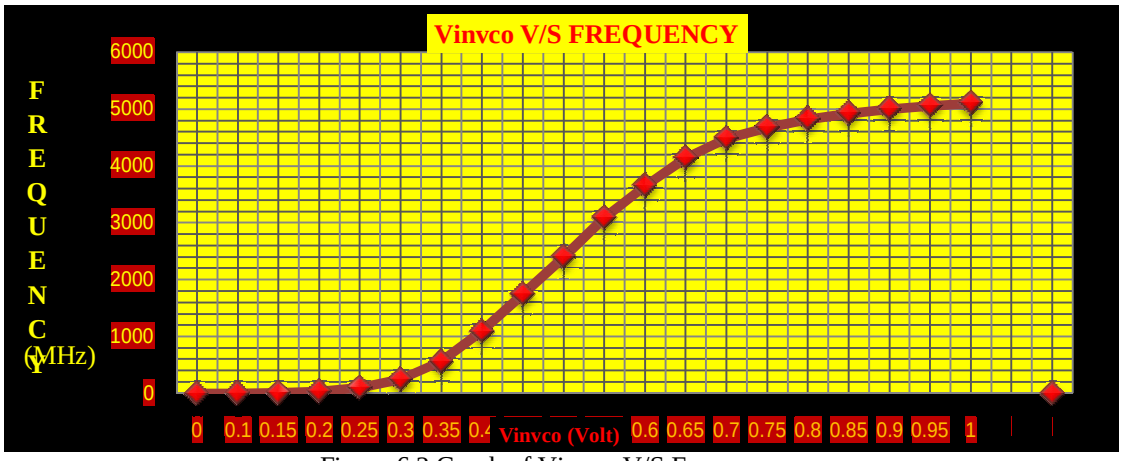

Figure 6.2 Graph of Vinvco V/S Frequency

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F. Programmable Frequency Divider

The Programmable frequency divider consists of a dual-modulus prescaler (DMP), a programmable (P) counter and a swallow (S) counter. The dual-modulus prescaler is based on both synchronous and asynchronous divider which scales the input frequency to a lower frequency to ease the complexity of asynchronous resettable modulo-Pand modulo-Scounters. In this technique, *S* input pulses are swallowed in the preceding arrangement such that the output period becomes longer by Sreference periods. In the initial state, the modulus control (MC) signal remains at logic '0' and allows the DMP to operate in the divide-by-(N+1) mode and the programmable P-counter and swallow S-counter are loaded to their initial states Since P>S, the S-counter reaches the final state earlier than P-counter and the end-of-count logic of the S-counter changes the MCto logic '1' allowing the DMP to switch to divide-by-*N* mode where the P-counter counts the remaining (P-S) input periods of 'N'. Thus the total division ratio is given by

Fout = ((N+1)S + N(P -S)) fin =(NP+S) fin.

From the circuit topology view point, prescaler and presettable counters are often implemented using different logic families, owing to their different speed specifications and a level shifter is required after the DMP to compensate different voltage rails. The basic programmable frequency divider architecture is shown in figure 7.

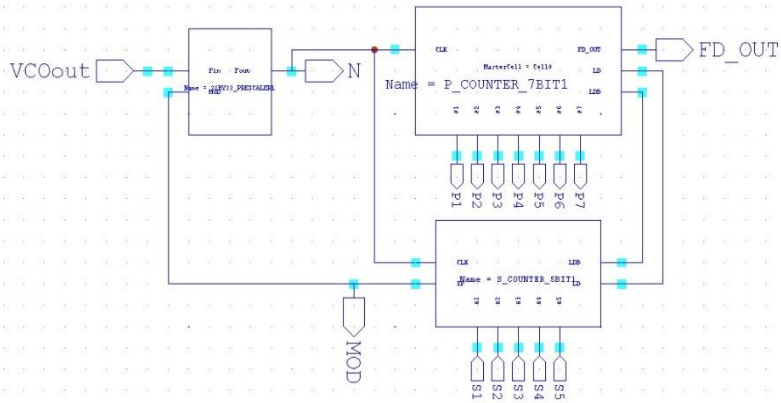

Figure7. Programmable Frequency Divider Architecture

Figure 7.1 Shows simulation result of Programmable Frequency Divider.VCO output frequency is 2.4GHz which is divided by programmable frequency divider and divide frequency by 2400 hence Div frequency is 1MHz.

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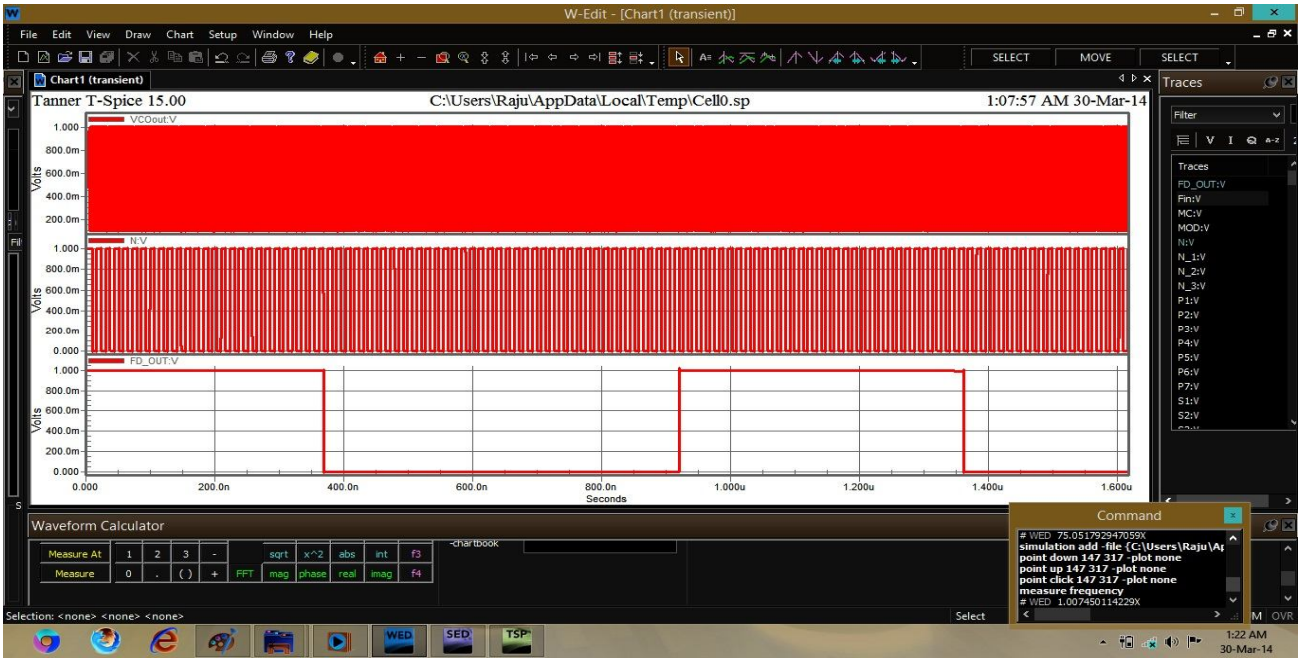

Figure7.1 simulation result of Programmable Frequency Divider

III. SIMULATIONS RESULTS OF THE SYNTHESIZER

The synthesizer has been simulated by using 45nm CMOS technology.The complete synthesizer draws 1.026 mW from a 1V voltage supply.

Figure 8.1 shows simulation result for P=71, S=1, Reference frequency is 1MHz and frequency division ratio is 2400 .VCO output Frequency observed is 2.44GHz

Figure8.1 simulation result for P=71,S=1,Ref=1MHz

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Figure 8.3 shows simulation result for P=71, S=31, Reference frequency is 1MHz and frequency division ratio is 2431 .VCO output Frequency observed is 2.54GHz

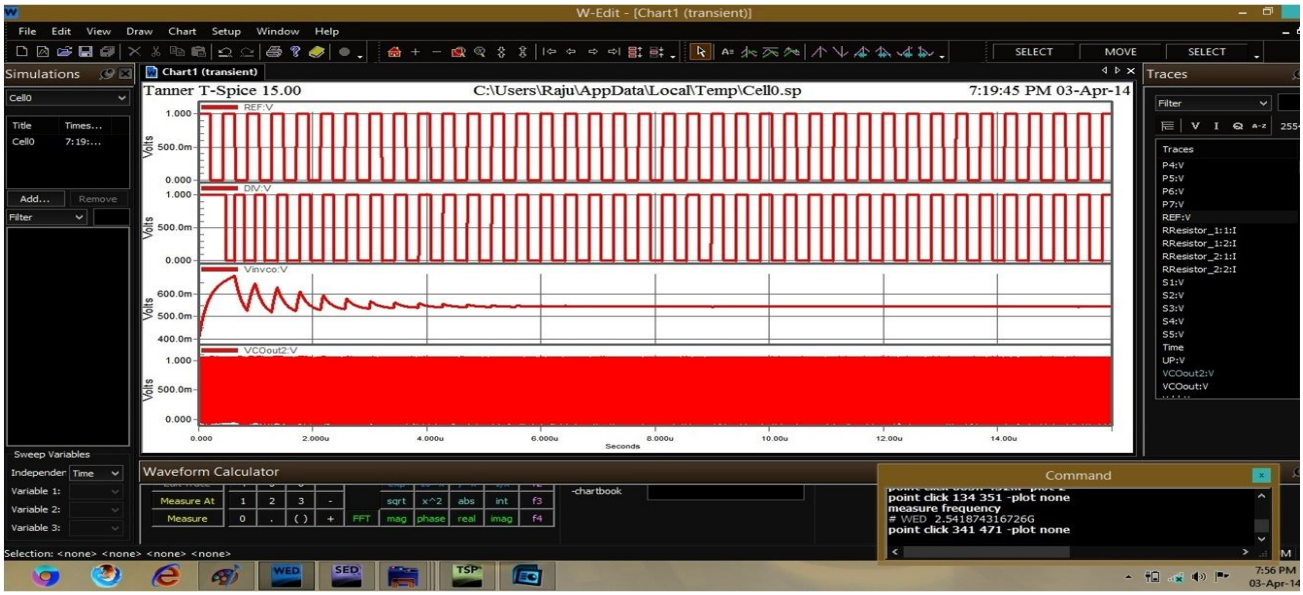

Figure8.2 simulation result for P=7,S=31,Ref=1MHz

VI. CONCLUSION

A fully integrated synthesizer has been presented for Bluetooth application. The design has been simulated in a standard 45nm CMOS technology. The VCO generates a center frequency at 2.4GHz at Vinco of 0.53V approximately. The PLL settles in approximately 4µs, generates frequencies from 2.44 to 2.54GHz in steps of 1MHz. The measured phase noise is -44.77 dBc/Hz at 1 MHz offset and the power consumption is 1.026 mW

TABLE I
Comparative Analysis of Synthesizer

Parameters	**Result of current work**	**Results Reported in [1]**		**Results Reported in [2]**	**Results Reported in [3]**	**Results Reported in [4]**
Technology	45nm	45nm	65nm	90nm	0.35µm	0.180µm
Supply voltage	1V	1.1V	1.2V	-	3.3V	1.2V
Frequency Rang.	2.46-2.54GHz	1.2 -2.4 GHz	3.5 – 5GHz	0.432GHz	2.4-2.479GHz	2.17-2.24GHz
Lock Time	4µs	-	-	-	100µs	-
Ref. Frequency	1MHz	2MHz	0.2MHz	27MHz	1MHz	1MHz
Phase Noise	-44.77dBc/Hz	-95dBc/Hz @1MHz	-119dBc/Hz @1MHz	-102dBc/Hz	-128dBc/Hz @3MHz	-112.77dBc/Hz
Power Dissipation	1.026mw	5.4mw	1.2mw	7mw	32.6mw	1.85mw

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BIOGRAPHY

Mr.Rajesh A. Dabhi received the Degree in Electronics and Communication Engineering from Saurashtra University, Rajkot & pursuing M.E. Degree in Electronics and Communication Engineering from Gujarat Technological University, Ahmedabad.

Mr.B.H.Nagpara received the Degree in Electronics and Communication Engineering from Saurashtra University, Rajkot & M.E. Degree in Electronics and Communication Engineering from Gujarat Technological University, Ahmedabad. Currently he is working as an Assistant Professor in Electronics & Communication at C.U.Shah University, Wadhwancity. His interests are in Digital System Design using VLSI/CMOS Technology, Analog and Mixed mode Designs.